Japanese Journal of Applied Physics
Vol. 46, No. 12, 2007, pp. 7654–7661
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Phonon-Limited Electron Mobility Behavior and Inherent Mobility Reduction Mechanism of Ultrathin Silicon-on-Insulator Layer with (111) Surface and Ultrathin Germanium-on-Insulator Layer with (001) Surface

Tsuyoshi YAMAMURA, Shingo SATO, and Yasuhisa OMURA

ORDIST and Graduate School of Engineering, Kansai University, 3-3-35 Yamate-cho, Suita, Osaka 564-8680, Japan

(Received June 27, 2007; accepted September 12, 2007; published online December 6, 2007)

One-dimensional self-consistent calculations and relaxation time approximations are used to study the phonon-limited electron mobility behavior of the inversion layer at room temperature for ultrathin body Si(111) and Ge(001) layers in single-gate (SG) and double-gate (DG) silicon-on-insulator (SOI) and germanium-on-insulator (GOI) metal–oxide–semiconductor (MOS) field-effect transistors (FETs). Assuming a 5-nm-thick SOI layer, it is shown that intravalley phonon scattering (acoustic-phonon scattering) in the DG SOI MOSFET inversion layer is strongly suppressed within a range of medium and high effective field (E_{eff}) values; DG SOI MOSFETs have higher phonon-limited electron mobility than SG SOI MOSFETs. Many simulations strongly indicate that, for medium E_{eff} values, the suppression of acoustic-phonon scattering in a 5-nm-thick DG SOI MOSFET primarily stems from the reduction of the form factor (F_{00}) value. Although similar phenomena are observed in approximately 7-nm-thick GOI layers with a Ge(001) surface, it is shown that there is little merit in using the Ge(001) surface for DG GOI MOSFETs. [DOI: 10.1143/JJAP.46.7654]

KEYWORDS: double gate, mobility enhancement, FinFET, ultrathin silicon, ultrathin germanium, phonon scattering, acoustic phonon, Si(111) surface, Ge(001) surface

1. Introduction

The phonon-limited electron mobility on the Si(001) surface of ultrathin-body (UTB) single-gate (SG) and double-gate (DG) silicon-on-insulator (SOI) metal–oxide–semiconductor field-effect transistors (MOSFETs) has been widely analyzed,[1–5] and its merits are well known. Recently, the electron mobility on the (110) Si surface of SG and DG SOI MOSFETs has been analyzed, and various strain techniques have been proposed and experimentally verified.[6,7] However, the results obtained using these techniques are not always reproducible, and the fabrication costs are high because strain device fabrication requires new fabrication processes and/or materials. We consider that another approach is required to improve the performance of UTB DG SOI MOSFETs or FinFETs.[8]

In the case of UTB SG and DG SOI MOSFETs, Esseni *et al.* showed the measured electron mobility results on the Si(001) surface;[9] their results using devices with a sub-10-nm-thick SOI layer show a slight improvement in the electron mobility of DG devices at room temperature. However, the effect of surface roughness on the electron mobility of SG and DG devices is not very clear. Esseni *et al.* also performed theoretical simulations on the electron mobility of SG and DG SOI MOSFETs on a Si(001) surface.[3] They investigated the effect of surface optical (SO) phonons[10] on the electron mobility of a UTB SOI layer to reproduce the measurements[11] of electron mobility dependence on SOI layer thickness (T_{SOI}). They stated the importance of the contributions of SO phonons and surface roughness scattering as mechanisms that could explain, to some extent, the somewhat low electron mobility measured in the experiments; however, they did not give a conclusive description because a thorough verification was not possible.

As mentioned previously, FinFETs are frequently fabricated on Si substrates with a (011) surface, where the inversion channel is formed on a Si(111) surface.[8] Although, so far, the Si(111) surface has not been well utilized because of its low mobility, the excellent chemical stability of the Si(111) surface should be noted because it simplifies the fabrication of thin Si devices.[12,13] Thus, the application of the Si(111) surface to a FinFET on a (011) substrate is not simply a theoretical discussion.

In this paper, we examine various behaviors and the reduction mechanism of the phonon-limited electron mobility of DG and SG SOI MOSFETs with a (111) Si surface for SOI layer thicknesses (T_{SOI}) ranging from 30 to 1 nm; the features of the phonon-limited electron mobility of DG and SG germanium-on-insulator (GOI) MOSFETs with a (001) Ge surface are also investigated because such surfaces have band structures fundamentally different from Si equivalents. Self-consistent simulations are performed assuming intravalley and intervalley scattering. Phonon-limited electron mobility behaviors of SG and DG SOI (GOI) MOSFETs are compared. Phonon-limited electron mobility behaviors and the reduction mechanism, which depend on materials and device structures, are examined by a detailed review of simulation results.

2. Simulation Model

The simulations assume SG and DG n-channel SOI (or GOI) MOSFETs. It is further assumed that the gate oxide thickness (T_{ox}) of the SG and DG SOI (or GOI) MOSFETs is 3 nm and the buried oxide layer thickness (T_{BOX}) of the SG SOI (or GOI) MOSFET is 200 nm. Impurity concentrations (N_{A}) in the SOI layer (or GOI layer) and Si (or Ge) substrate are considered to be $5 \times 10^{15}\,\mathrm{cm}^{-3}$. In this paper, we simulate the phonon-limited electron mobility in the inversion layers of SG and DG SOI (or GOI) MOSFETs on (111) Si [or (001) Ge] surfaces at 300 K using a relaxation time approximation on the basis of a one-dimensional self-consistent solution of the Schrödinger and Poisson equations; the physical parameters assumed in the simulations are shown in previous reports;[4,14–17] the assumed electron masses are listed in Table I for Si(001) and II for Ge(001). Electron mobility is derived using the following formula

Table I. Electron effective mass values in Si (X band) assumed in simulations.[17]

	Si(001) surface		Si(111) surface
	2-fold valley	4-fold valley	6-fold valley
m_z^*/m_0 (confinement)	0.916	0.190	0.258
Conductivity mass/m_0	0.190	0.315	0.296

Table II. Electron effective mass values in Ge(001) (L, X, and Γ bands) assumed in simulations.[17]

	Ge(001) surface			
	L valley	X valley (2-fold)	X valley (4-fold)	Γ valley
m_z^*/m_0 (confinement)	0.117	1.35	0.290	0.040
Conductivity mass/m_0	0.149	0.290	0.477	0.040

$$\mu_i = \frac{q\int (E - E_i)\tau_i(E)\frac{\partial f}{\partial E}\,dE}{m_{c,i}\int (E - E_i)\frac{\partial f}{\partial E}\,dE}, \quad (1)$$

where $m_{c,i}$ is the conductivity effective mass of electrons at the specific ith subband, $\tau_i(E)$ is the relaxation time of phonon scattering, and E_i is the ith subband energy level.

$E_{\rm eff}$ for the SG SOI (or GOI) MOSFET is defined as

$$E_{\rm eff} = \frac{\int_{z_0}^{T_{\rm SOI}} n(z)E(z)\,dz}{\int_{z_0}^{T_{\rm SOI}} n(z)\,dz}, \quad (2)$$

where $n(z)$ is the local electron density, $E(z)$ is the local transverse electric field, and z_0 is the position of the front semiconductor/insulator interface; in the case of GOI devices, $T_{\rm SOI}$ is replaced with $T_{\rm GOI}$. On the other hand, $E_{\rm eff}$ for the DG SOI (or GOI) MOSFET is defined as

$$E_{\rm eff} = \frac{\int_{z_0}^{T_{\rm SOI}/2} n(z)E(z)\,dz}{\int_{z_0}^{T_{\rm SOI}/2} n(z)\,dz}. \quad (3)$$

Integration is up to $T_{\rm SOI}/2$ (or $T_{\rm GOI}/2$) because we assume a symmetric DG SOI (or GOI) MOSFET; this means that half of the inversion carrier density of the DG MOSFET is the same as that of the SG MOSFET when the devices have identical $E_{\rm eff}$.

3. Results and Discussion

3.1 *Electron mobility on Si(111) surface*

The simulated phonon-limited electron mobility on the (111) surface is shown in Fig. 1 as a function of $T_{\rm SOI}$ for various $E_{\rm eff}$ values; the simulated mobility values of the DG and SG SOI MOSFETs are compared. It is seen that the DG SOI MOSFET offers superior mobility for $T_{\rm SOI}$ values ranging from 4 to 8 nm in a medium and high $E_{\rm eff}$ range; it is very important to note that DG SOI MOSFETs offer superior mobility over a range of medium and high $E_{\rm eff}$ values because modern MOSFETs usually operate under $E_{\rm eff}$ values higher than $1\,{\rm MV\,cm^{-1}}$. The mobility enhancement peaks at approximately $T_{\rm SOI} = 5$ nm for $E_{\rm eff} > 0.5\,{\rm MV\,cm^{-1}}$. It is known from simulations that the mobility of DG SOI MOSFETs with a (001) Si surface is superior in a low-$E_{\rm eff}$ range.[1-3] Previous reports on the simulated electron mobility of (001) Si surface inversion layers have indicated that SG SOI MOSFETs have higher electron mobility than DG SOI MOSFETs in the high-$E_{\rm eff}$ range ($\sim$1 MV cm^{-1}) for $T_{\rm SOI}$ values ranging from 2 to 5 nm;[1-3,5] at other $T_{\rm SOI}$, values, it is known that DG SOI MOSFETs have slightly higher electron mobility than SG SOI MOSFETs at low $E_{\rm eff}$ range ($\sim$0.1 MV cm^{-1}).[1,2] The expected phonon-limited electron mobility of a 5-nm-$T_{\rm SOI}$ DG SOI MOSFET with a (111) Si surface is 450 cm^2 V^{-1} s^{-1} at $E_{\rm eff} = 1\,{\rm MV\,cm^{-1}}$; this is about 85% of that of the equivalent DG SOI MOSFET with a (001) Si surface. This is the advantage of using the (111) Si side surface configuration in device applications such as FinFETs on (011) Si substrates[8] because the hole mobility superiority on the (011) Si surface has attracted attention recently.[18] In real devices, it is anticipated that surface-roughness scattering will strongly effect electron mobility;[9] however, advances in etching techniques will yield virtually flat surfaces in the future.[12,13,19] A related discussion is given in §3.3.

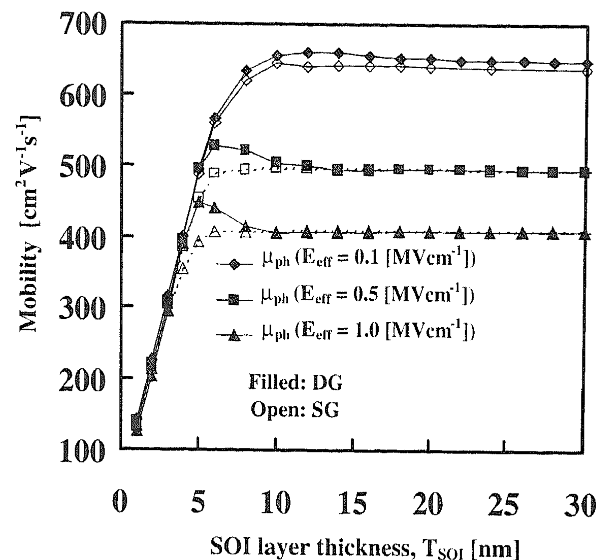


Fig. 1. $T_{\rm SOI}$ dependencies of simulated phonon-limited electron mobility with parameter of $E_{\rm eff}$. The mobility values of DG and SG MOSFETs with a (111) Si surface channel are compared.

The phonon-limited electron mobility on the (111) Si surface is shown as a function of $E_{\rm eff}$ for DG and SG SOI MOSFETs in Fig. 2; the parameter is $T_{\rm SOI}$. The electron mobility of the DG SOI MOSFET with 5 nm $T_{\rm SOI}$ exceeds that with 10 nm $T_{\rm SOI}$ for $E_{\rm eff} > 0.5\,{\rm MV\,cm^{-1}}$; in contrast, the SG SOI MOSFET does not exhibit such behavior. As shown in Fig. 2, the DG SOI MOSFET with 5 nm $T_{\rm SOI}$ has higher electron mobility than the SG SOI MOSFET for $E_{\rm eff} > 0.2\,{\rm MV\,cm^{-1}}$. These results are very interesting because they are not seen in SOI MOSFETs with the (001) Si surface at medium and high $E_{\rm eff}$ values.[2,3,5]

To consider the background to the suppression of intraband transitions, the occupation fraction of electrons in subbands is shown in Fig. 3 as a function of SOI layer thickness ($T_{\rm SOI}$) for a high $E_{\rm eff}$ of 1 MV cm^{-1}. Independently

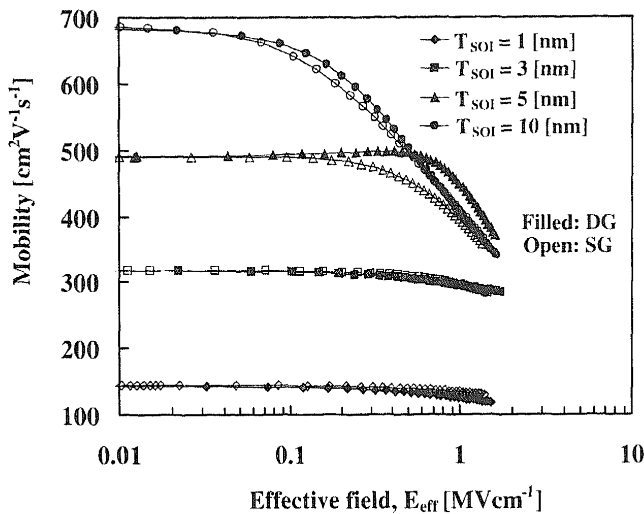


Fig. 2. E_{eff} dependencies of simulated phonon-limited electron mobility with parameter of T_{SOI}. The mobility values of DG and SG MOSFETs with a (111) Si surface channel are compared.

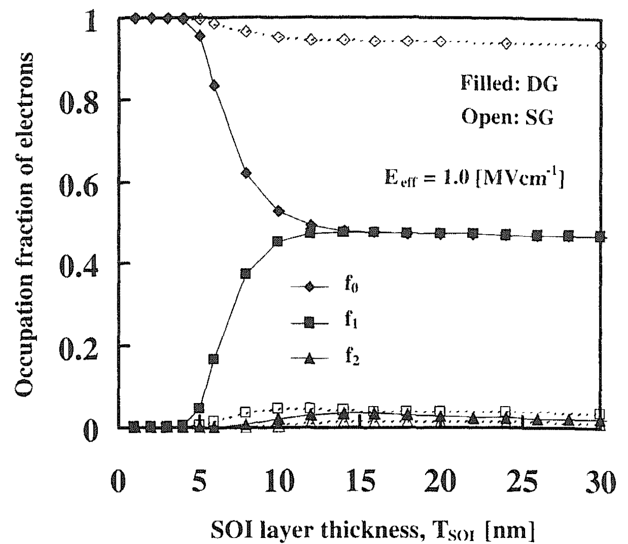


Fig. 3. Occupation fraction of electrons in subbands as a function of SOI layer thickness (T_{SOI}) for (111) Si surface under the high-field condition ($E_{eff} = 1\,\mathrm{MV\,cm^{-1}}$).

of the E_{eff} range and device type, it is seen that the occupation fraction at the lowest subband has quite a high value for $T_{SOI} < 6\,\mathrm{nm}$, although the occupation fraction at the lowest subband has a very high value regardless of T_{SOI} in SG SOI MOSFET. For a low E_{eff} of $0.1\,\mathrm{MV\,cm^{-1}}$, the occupation fraction at the lowest subband has quite a high value only for $T_{SOI} < 6\,\mathrm{nm}$ for SG and DG SOI MOSFET's (not shown here). This indicates that electrons at the lowest subband dominate the primary aspect of electron transport; this behavior of the occupation fraction is very similar to past simulation results for the Si(001) surface.[1]

Figure 4(a) shows the mobility of electrons sharing the lowest subband as a function of E_{eff} for 5-nm-T_{SOI} SG and DG SOI MOSFETs with a (111) Si surface channel; intraband-scattering-limited mobility (here, primarily acoustic-phonon scattering) ($\mu_{0,\mathrm{intra}}$) and interband-scattering-limited mobility (i.e., primarily optical-phonon scattering) ($\mu_{0,\mathrm{inter}}$) are also shown. It can be seen that the intraband transitions in the channel of the DG SOI MOSFET are strongly suppressed around the E_{eff} of $10^6\,\mathrm{V\,cm^{-1}}$. Figure 4(a) also suggests that the interband scattering (primarily optical-phonon scattering) of electrons sharing the lowest subband is not suppressed at high E_{eff} values in SG and DG SOI MOSFETs. In Fig. 4(a), it is seen that the total mobility of electrons sharing the lowest subband is around $500\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Thus, as shown in Fig. 4(b), we examined the magnitude of the electron mobility in devices sharing higher subbands (μ_1 and μ_2) with a 5 nm T_{SOI}. Both μ_1 and μ_2 are almost insensitive to E_{eff} for $E_{eff} < 2\,\mathrm{MV\,cm^{-1}}$, and their values are at most $600\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, which suggests that μ_0 predominantly contributes to the total mobility. Finally, we show the wave functions of electrons sharing the lowest subband at E_{eff} values of 0.1 and 1 MV $\mathrm{cm^{-1}}$ for devices with a 5 nm T_{SOI} in Figs. 4(c) and 4(d). Figure 4(c) shows that the wave function of the SG SOI MOSFET with a 5 nm T_{SOI} is localized very near the gate oxide for $E_{eff} = 1\,\mathrm{MV\,cm^{-1}}$, and Fig. 4(d) shows that the wave function of the DG SOI MOSFET with a 5 nm T_{SOI} is localized around the center of the SOI layer independently of E_{eff}. The surface localization of the wave function of the SG SOI MOSFET basically enhances the scattering probability because of the uncertainty principle. On the other hand, the semiflat profile of the DG SOI MOSFET wave function suggests lower scattering probability because there are few transitions from the lowest to the second subband [see Fig. 5(a)].

Because the, form factor (F_{ij}) affects the probability of a transition from subband i to j, Fig. 5 shows the E_{eff} dependencies of the F_{ij} of electrons sharing the various subbands for 5 nm-T_{SOI} SG and DG SOI MOSFETs for comparison; Fig. 5(a) is for electrons on the (111) Si surface, Fig. 5(b) is for electrons sharing the 4-fold valleys on the (001) Si surface, and Fig. 5(c) is for electrons sharing the 2-fold valleys on the (001) Si surface. In Fig. 5(a), for the (111) Si surface, we can see that F_{00} of the DG SOI MOSFET drops around the E_{eff} of $10^6\,\mathrm{V\,cm^{-1}}$, while F_{01} slightly increases around the E_{eff} of $10^6\,\mathrm{V\,cm^{-1}}$; the decrease in F_{00} indicates suppression of the intra-subband transition of electrons sharing the lowest subband; $\mu_{0,\mathrm{intra}}$ of the DG SOI MOSFET increases around the E_{eff} value of $10^6\,\mathrm{V\,cm^{-1}}$. On the other hand, we can see that F_{00} of the SG SOI MOSFET markedly increases around the E_{eff} of $10^6\,\mathrm{V\,cm^{-1}}$, while F_{01} decreases around the E_{eff} of $10^6\,\mathrm{V\,cm^{-1}}$; this results in the decrease in $\mu_{0,\mathrm{intra}}$ of electrons sharing the lowest subband in the SG SOI MOSFET around the E_{eff} of $10^6\,\mathrm{V\,cm^{-1}}$. In contrast to F_{00} and F_{01}, F_{11} and F_{22} are almost insensitive to E_{eff}; because the occupation fractions of the first and the second excited states are small, the contribution of the mobility values of electrons sharing them is very small. Now, acoustic-phonon scattering of the lowest-subband electrons is well suppressed around the E_{eff} value of $10^6\,\mathrm{V\,cm^{-1}}$ for the 5-nm T_{SOI} DG SOI MOSFET on the (111) Si surface as seen in Fig. 4. However, the suppression of acoustic-phonon scattering becomes modest at high E_{eff} values because the decrease in subband-to-subband energy difference promotes the transition between the lowest subband and the second subband, as is anticipated from the increase in F_{01} at high E_{eff} values.[1,2] Therefore, it can be considered that the suppression of acoustic-phonon

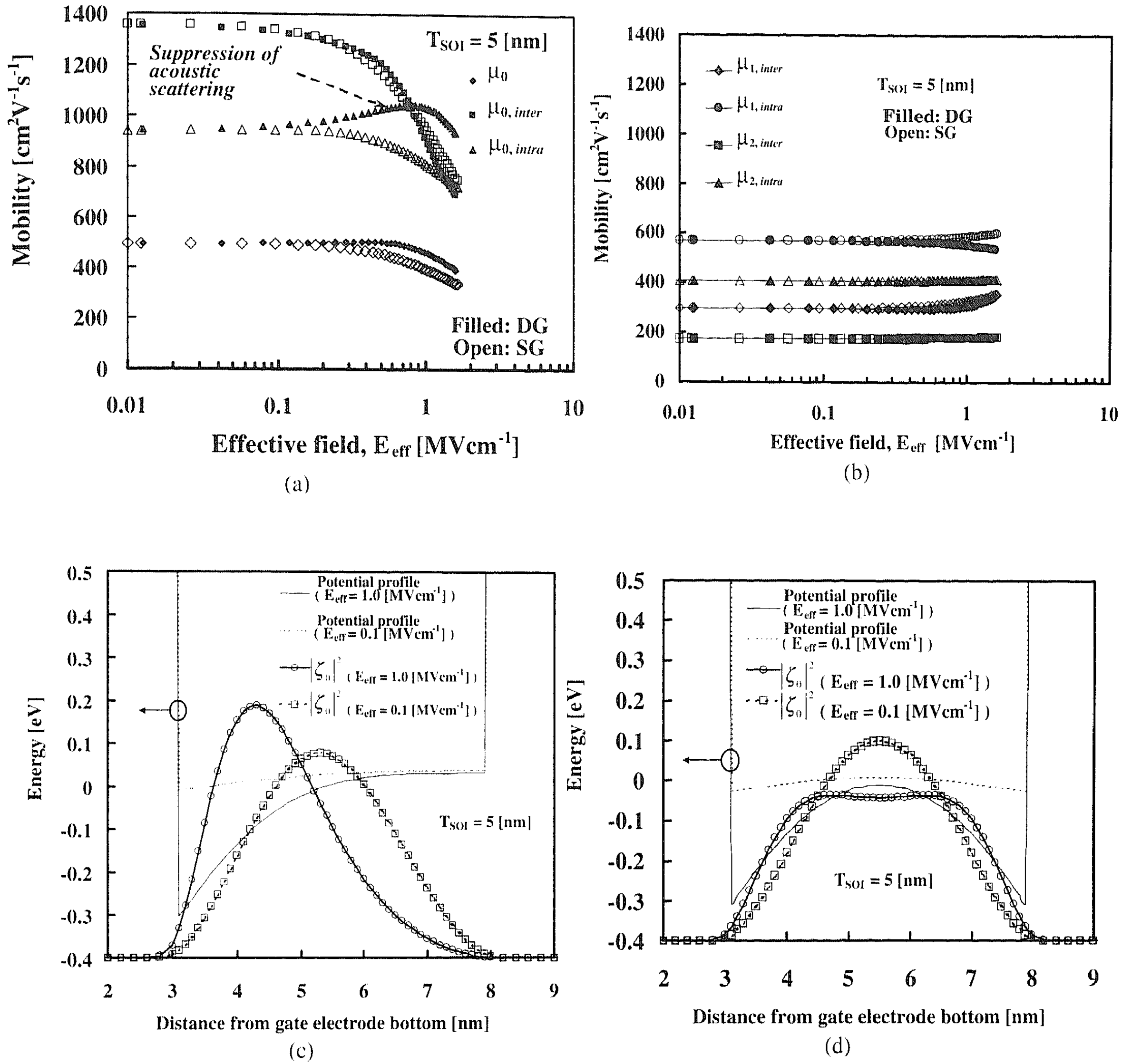
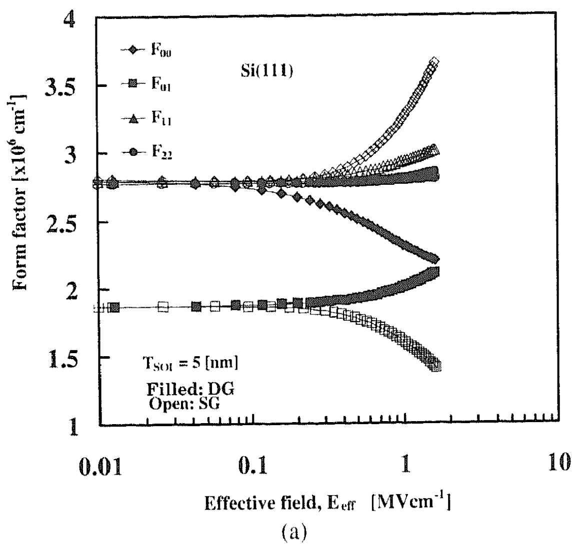


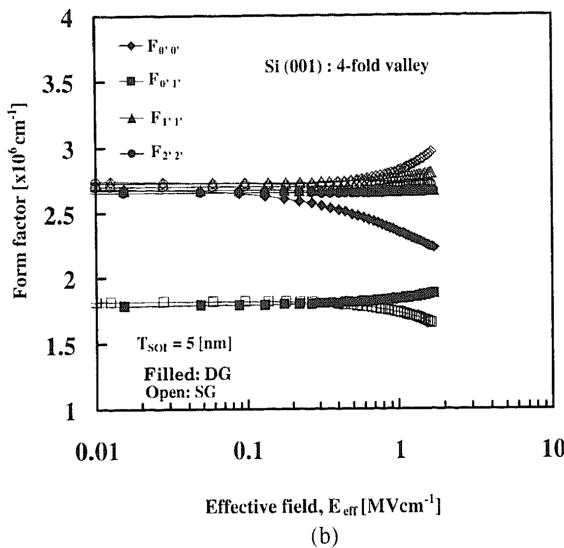
Fig. 4. E_{eff} dependencies of lowest- and second-subband phonon-limited electron mobility. The intravalley-scattering-limited mobility ($\mu_{0,intra}$) and intervalley-scattering-limited mobility ($\mu_{0,inter}$) are shown separately for SG and DG SOI MOSFETs with a (111) Si surface channel; μ_0 is total mobility including $\mu_{0,intra}$ and $\mu_{0,inter}$. For consideration, wave functions of the lowest subband for SG and DG SOI MOSFETs are also shown at $E_{eff} = 0.1$ and $1\,MV\,cm^{-1}$. (a) E_{eff} dependencies of lowest-subband phonon-limited electron mobility. (b) E_{eff} dependencies of second-subband phonon-limited electron mobility. (c) Wave functions of lowest subband for SG SOI MOSFET at $E_{eff} = 0.1$ and $1\,MV\,cm^{-1}$. (d) Wave functions of lowest subband for DG SOI MOSFET at $E_{eff} = 0.1$ and $1\,MV\,cm^{-1}$.

scattering in the 5 nm-T_{SOI} DG SOI MOSFET primarily stems from a decrease in F_{00} at medium E_{eff} values.

On the other hand, Figs. 5(b) and 5(c) show the E_{eff} dependencies of the form factors of electrons sharing the 4- and 2-fold valleys on the (001) Si surface for 5 nm-T_{SOI} SG and DG SOI MOSFETs for comparison, respectively. In the case of the 4-fold valley on the (001) Si surface, the $F_{0'0'}$ of the DG SOI MOSFET decreases for $E_{eff} > 0.2\,MV\,cm^{-1}$, while $F_{0'1'}$ decreases to a low level independently of E_{eff}. On the other hand, the $F_{0'0'}$ of the SG SOI MOSFET significantly increases for $E_{eff} > 1\,MV\,cm^{-1}$, while the $F_{0'1'}$ decreases slightly for $E_{eff} > 1\,MV\,cm^{-1}$. This apparently suggests a high electron mobility of the DG SOI MOSFET in the high-E_{eff} range. However, it is anticipated that electrons sharing the 4-fold valleys do not primarily affect the total mobility value because of its low occupation fraction. In contrast, the occupation fraction of the 2-fold valley on the (001) Si surface is very high. In Fig. 5(c), it is seen that the F_{00} of the DG SOI MOSFET decreases for $E_{eff} > 0.1\,MV\,cm^{-1}$ and recovers for $E_{eff} > 1\,MV\,cm^{-1}$. In addition, the F_{01} of the DG SOI MOSFET rapidly increases for $E_{eff} > 0.1\,MV\,cm^{-1}$. In the SG SOI MOSFET, F_{00} rapidly increases for $E_{eff} > 0.1\,MV\,cm^{-1}$, while F_{01} decreases for $E_{eff} > 0.1\,MV\,cm^{-1}$. This suggests that there is no mobility enhancement of the SOI MOSFET on the (001) Si surface in the high-E_{eff} range.

In Fig. 2, it can be seen that the electron mobility of SG and DG SOI MOSFETs with 10 nm T_{SOI} on the (111) Si surface is higher than that of devices with 5 nm T_{SOI} in the low-E_{eff} range, while the electron mobility of SG and DG SOI MOSFETs with 10 nm T_{SOI} is lower than that of devices with 5 nm T_{SOI} in the high-E_{eff} range. To more fully discuss this point, the E_{eff} dependence of the form factor (F_{ij}), which affects the probability of transition from subband i to j, is shown in Fig. 6 for two DG SOI MOSFETs with different T_{SOI} values ($T_{SOI} = 5$ and 10 nm) on the (111) Si surface. In Fig. 7, relaxation time, defined by acoustic-phonon scattering in a 5-nm-T_{SOI} DG SOI MOSFET, and the energy





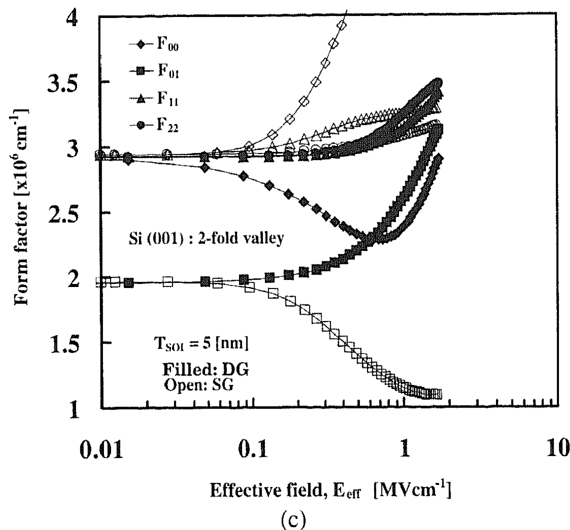


Fig. 5. $E_{\rm eff}$ dependencies of form factors of electrons sharing various subbands for 5 nm-$T_{\rm SOI}$ SG and DG SOI MOSFETs for (111) and (001) Si surfaces. (a) Form factors for (111) Si surface. (b) Form factors of 4-fold valley for (001) Si surface. (c) Form factors of 2-fold valley for (001) Si surface.

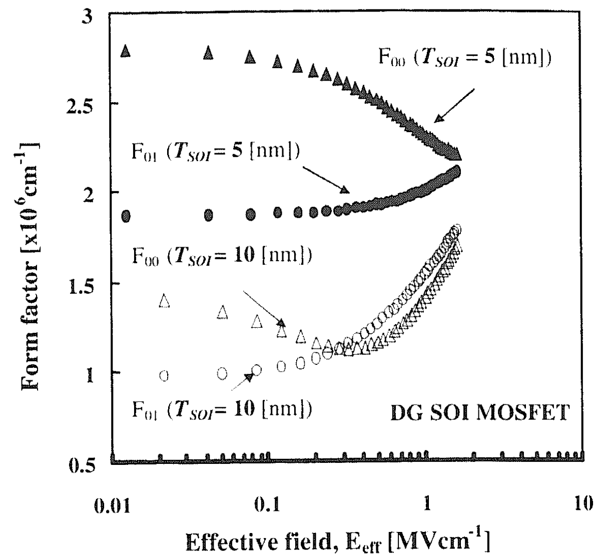


Fig. 6. $E_{\rm eff}$ dependence of form factor (F_{ij}), which affects the probability of transition from subband i to j, for two DG SOI MOSFETs with different $T_{\rm SOI}$ values ($T_{\rm SOI}$ = 5 and 10 nm) for (111) Si surface.

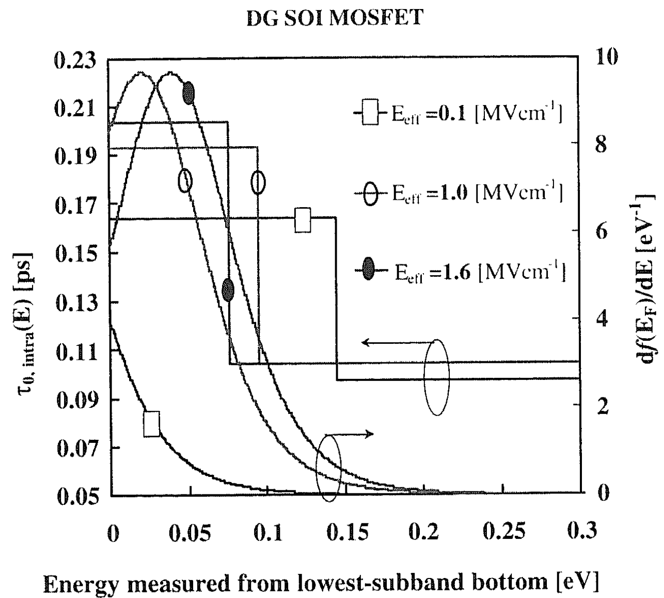


Fig. 7. Relaxation time, defined by acoustic-phonon scattering in a 5-nm-$T_{\rm SOI}$ DG SOI MOSFET, and the energy derivative of the Fermi–Dirac function ($df(E_{\rm F})/dE$) as a function of electron energy measured from the ground state for various $E_{\rm eff}$ values for Si(111) surface.

derivative of the Fermi–Dirac function ($df(E_{\rm F})/dE$) are shown as functions of electron energy measured from the lowest-subband bottom for various $E_{\rm eff}$ values. The F_{00} of a 5-nm-$T_{\rm SOI}$ device decreases as $E_{\rm eff}$ increases (see Fig. 6), which results in the suppression of acoustic-phonon scattering for the lowest-subband electrons; however, the suppression of acoustic-phonon scattering becomes modest at high $E_{\rm eff}$ values because the decrease in the subband-to-subband energy difference promotes the transition between the lowest subband and the second subband as anticipated from Fig. 7. Becasue a high $df(E_{\rm F})/dE$ at a low energy suggests that electrons strongly contribute to the suppression of scattering events, we can see that the condition of $E_{\rm eff} = 1\,{\rm MV\,cm^{-1}}$ yields high mobility. On the other hand, as seen in Fig. 6 for the 10 nm $T_{\rm SOI}$, both F_{00} and F_{01} rapidly increase as $E_{\rm eff}$ increases in the high-$E_{\rm eff}$ range, which lowers the electron mobility in the high-$E_{\rm eff}$ range; the lowest subband transitions as well as the subband-to-subband transitions increase in the high-$E_{\rm eff}$ range. Therefore, the subband

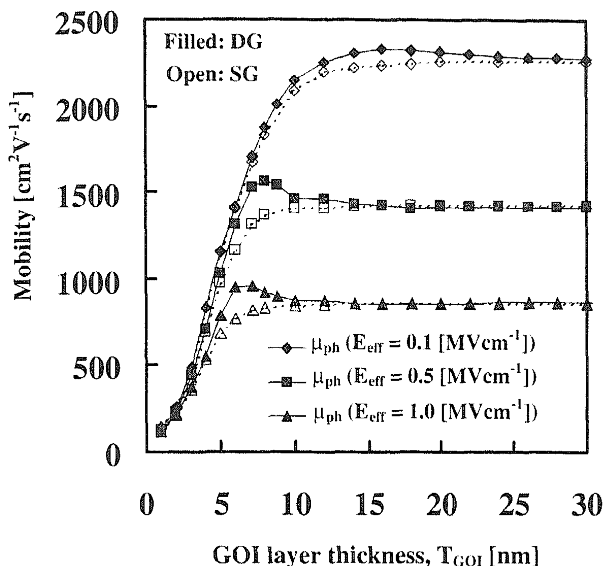


Fig. 8. Simulated phonon-limited electron mobility on the (001) Ge surface as a function of T_{GOI} for various E_{eff} values; simulated mobility values of the DG and SG GOI MOSFETs are compared.

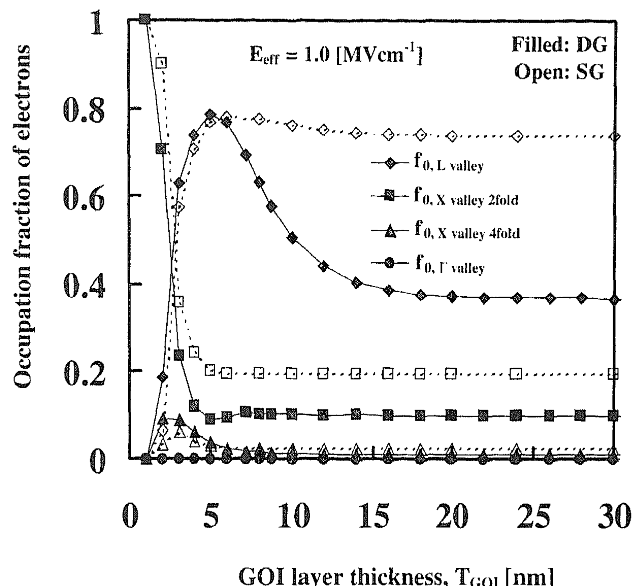


Fig. 9. Occupation fraction of electrons in lowest subband as a function of GOI layer thickness (T_{GOI}) for L, X (2-fold and 4-fold), and Γ valleys at $E_{eff} = 1\,\mathrm{MV\,cm^{-1}}$. A (001) Ge surface is assumed.

structure plays an important role in the suppression of phonon scattering.[1,2,5)]

3.2 *Electron mobility on (001) Ge surface*

From the above simulation results, we would expect that a similar phenomenon occurs in a GOI layer on the Ge(001) surface because the conduction-band location on the Ge(001) surface resembles that on the Si(111) surface. We performed self-consistent simulations using known physical parameters and the effective masses listed in Table II; note that we have to consider X and L valleys in a GOI layer on the (001) Ge surface. In a past paper,[20)] the electron mobility of the SG GOI MOSFET is discussed on the basis of simulation results, not that of the DG GOI MOSFET. Thus, we compare the electron mobility of the SG GOI MOSFET with that of the DG GOI MOSFET in the following.

The simulated phonon-limited electron mobility on the (001) surface is shown in Fig. 8 as a function of T_{GOI} for various E_{eff} values; the simulated mobility values of the DG and SG GOI MOSFETs are compared. It is seen that the DG GOI MOSFET offers superior mobility for T_{GOI} values ranging from 7 to 8 nm in a medium- and high-E_{eff} range. Maximal mobility enhancement appears at approximately $T_{GOI} = 7\,\mathrm{nm}$ for $E_{eff} > 0.4\,\mathrm{MV\,cm^{-1}}$.

It is seen that that E_{eff} dependence of phonon-limited electron mobility on the (001) Ge surface (not shown here) is identical to that on the (111) Si surface shown in Fig. 2, where the electron mobility of the DG GOI MOSFET with 7.2 nm T_{SOI} exceeds that with 10 nm T_{GOI} for $E_{eff} > 0.5\,\mathrm{MV\,cm^{-1}}$; in contrast, the SG GOI MOSFET does not exhibit such behavior. It is found that the DG GOI MOSFET with 7.2 nm T_{GOI} has higher electron mobility than the SG GOI MOSFET for $E_{eff} > 0.1\,\mathrm{MV\,cm^{-1}}$.

Figure 9 shows the occupation fraction of the lowest subband for L, X (2- and 4-fold), and Γ valleys as a function of T_{GOI} for $E_{eff} = 1\,\mathrm{MV\,cm^{-1}}$; the occupation fraction of the lowest subband in the low-E_{eff} range is not shown here because it is almost the same as that for $E_{eff} = 1\,\mathrm{MV\,cm^{-1}}$. It is seen that the occupation factor of the lowest subband (f_0) of the L valley takes a maximum value at approximately $T_{GOI} = 7\,\mathrm{nm}$, and is almost independent of E_{eff}. At $E_{eff} = 1\,\mathrm{MV\,cm^{-1}}$, f_0 of the L valley around $T_{GOI} = 7\,\mathrm{nm}$ is reduced and f_0 of the X valley (2-fold) around $T_{GOI} = 7$ nm increases relative to that in the low-E_{eff} range. The occupation fraction (f_0) of the X valley (2-fold) in the SG GOI MOSFET is higher than that in the DG GOI MOSFET at $E_{eff} = 1\,\mathrm{MV\,cm^{-1}}$; this represents a disadvantage for SG GOI MOSFETs because of the high effective mass. It follows that the phonon-limited electron mobility of DG GOI MOSFETs should be better than that of SG GOI MOSFETs in the high-E_{eff} range.

Figure 10 shows the phonon-limited mobility of electrons sharing the lowest subband of various valleys (L and X valleys) at $E_{eff} = 1\,\mathrm{MV\,cm^{-1}}$. In the case of the L valley, the electron mobility of DG GOI MOSFETs is better than that of SG GOI MOSFETs, although the T_{GOI} at which the mobility is superior appears to be restricted to a range of small T_{GOI} values. The phonon-limited mobility of electrons sharing the lowest subband of the 2-fold X valley of DG GOI MOSFETs is better than that of SG GOI MOSFETs; unlike the case of the L valley, this superiority holds for $T_{GOI} > 2\,\mathrm{nm}$ independently of E_{eff}. The phonon-limited mobility of electrons sharing the lowest subband of the 4-fold X valley of DG GOI MOSFETs is better than that of SG GOI MOSFETs; unlike the case of the L valley, the clear electron mobility superiority of DG GOI MOSFETs holds for $T_{GOI} >$ 1 nm independently of E_{eff}. From Fig. 9, we can see that the mobility superiority of DG GOI MOSFETs stems from the physical properties of the electrons sharing the L valley.

Intraband-scattering-limited mobility ($\mu_{0,\mathrm{intra}}$), interband-scattering-limited mobility (primarily the optical-phonon scattering) ($\mu_{0,\mathrm{inter}}$), and the total phonon-limited mobility of electrons sharing the L valley are shown in Fig. 11 for SG and DG GOI MOSFETs with a (001) Ge surface channel for $T_{GOI} = 7.2\,\mathrm{nm}$. It can be seen that the intraband transitions in the DG GOI MOSFETs channel are strongly suppressed for $E_{eff} > 0.2\,\mathrm{MV\,cm^{-1}}$. Figure 11 also shows that the

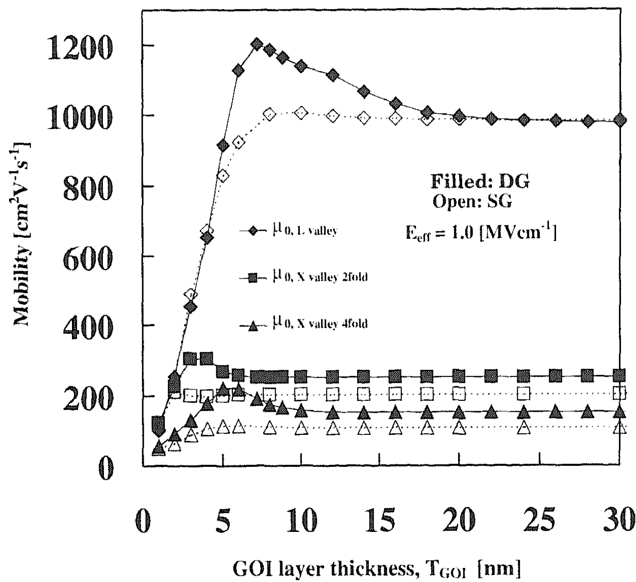


Fig. 10. Simulated phonon-limited mobility of electrons sharing L valley, 2-fold X valley, and 4-fold X valley on (001) Ge surface as a function of T_{GOI} at $E_{eff} = 1\ MV\,cm^{-1}$.

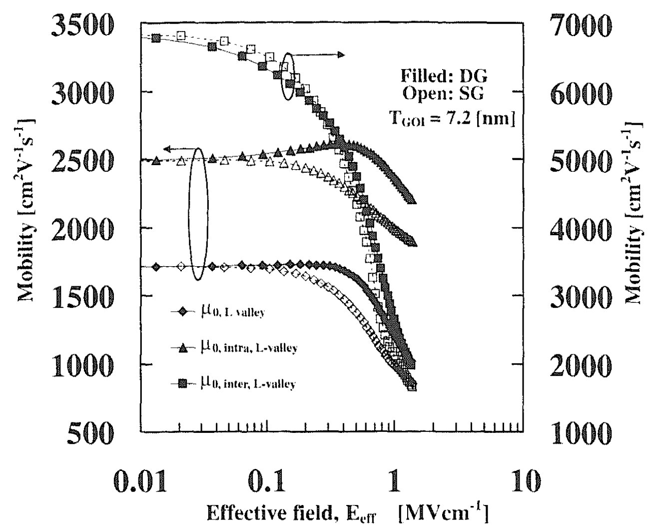


Fig. 11. Intraband-scattering-limited mobility ($\mu_{0,intra}$), interband-scattering-limited mobility ($\mu_{0,inter}$), and total phonon-limited mobility of electrons sharing the L valley for SG and DG GOI MOSFETs with (001) Ge surface channel for $T_{GOI} = 7.2$ nm.

interband scattering of electrons sharing the lowest subband is also slightly suppressed at high E_{eff} values in the DG GOI MOSFET. However, Fig. 11 suggests that the suppression of intraband scattering contributes more to mobility enhancement than that of interband scattering. These behaviors are slightly different from the case of the Si(111) surface because the transport in Ge is affected moderately by optical-phonon-induced intervalley scattering events. Physical parameters for the X-valley electrons of Si and the L-valley electrons of Ge (such as deformation potential values for acoustic-phonon scattering and optical-phonon scattering) are identical to each other. Thus, it is anticipated that the electron mobility difference between Si and Ge primarily stems from the effective mass value.

3.3 *Progress of discussion on mobility reduction in ultrathin body field-effect transistors*

In the case of MOSFETs with an ultrathin SOI (or GOI) layer, the local-thickness-fluctuation-induced (LTFI) scattering must be considered as well as the conventional surface roughness scattering because the LTFI scattering event cannot be neglected in sub-10-nm-thick layers.[21] In addition, Koga *et al.* demonstrated that Coulomb scattering due to charged centers at the buried-oxide interface may degrade the mobility with decreasing SOI thickness, unless the SOI wafer quality at the buried-oxide interface is controlled carefully.[22] The physical model is still controversial because no comprehensive fluctuation model that is based on local thickness fluctuation has been established. A more accurate model is required. In addition, the first-principles approach for SOI and GOI structures demonstrates the dependence of the effective mass on layer thickness.[23] The study suggests that the electron mobility of the GOI layer must be reconsidered for layers less than 10-nm thick.[24]

The acoustic-phonon confinement effect has recently been studied[25] because the conventional matrix element of phonon scattering is calculated assuming the bulk phonon mode.[10,15,17] It has been shown that confined acoustic phonons enhance the scattering, and that they degrade the phonon-limited electron mobility by about 30% in the T_{SOI} range of 5–10 nm;[25] we note that the surface orientation dependence of the acoustic phonon confinement was not considered, so its quantitative effect is not clear.

It has been suggested that the surface optical (SO) phonon mode[3,10] degrades electron mobility when a high-k gate insulator is used because of the large difference between the static and optical permittivities in high-k gate insulators.[3] It is estimated that SO phonons primarily enable inter-subband transitions in the T_{SOI} range of sub-10 nm. Esseni *et al.* demonstrated the impact of SO phonons on the electron mobility of ultrathin SOI MOSFETs.[3]

As described above, some recent papers suggest the necessity of further study on the impact of phonon scattering events on carrier mobility. Because this paper has discussed the fundamental aspects of phonon-limited electron mobility, we consider that the present prediction still holds meaningfulness.

4. Conclusions

One-dimensional self-consistent calculations and relaxation time approximations were used to study the phonon-limited electron mobility of the inversion layer at room temperature for ultrathin-body Si(111) and Ge(001) layers in single-gate (SG) and double-gate (DG) silicon-on-insulator (SOI) and germanium-on-insulator (GOI) metal–oxide–semiconductor field-effect transistors (MOSFETs). Assuming a 5-nm-thick SOI layer, it has been demonstrated that intravalley phonon scattering (acoustic-phonon scattering) in the DG SOI MOSFET inversion layer is strongly suppressed within a range of medium and high effective field (E_{eff}) values; DG SOI MOSFETs have higher phonon-limited electron mobility than SG SOI MOSFETs. Many simulations strongly indicated that the suppression of acoustic-phonon scattering in a 5-nm-thick DG SOI MOSFET primarily stems from the reduction of the form factor (F_{00}) at medium E_{eff} values. Similar phenomena were observed in about 7-nm-thick GOI layers with a Ge(001) surface, although the

transport is also affected by optical-phonon-induced intervalley scattering in Ge.

Acknowledgment

Part of the computations made in this research were performed on the Large-Scale Computer System at the Osaka University Cyber-Media Center.

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