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Adhesion–delamination phenomena at the surfaces and interfaces in microelectronics and MEMS structures and packaged devices

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Abstract

Physico-chemical mechanisms of adhesion and debonding at the various surfaces and interfaces of semiconductor devices, integrated circuits and microelectromechanical systems are systematically examined, starting from chip manufacturing and traversing the process stages to the ultimate finished product. Sources of intrinsic and thermal stresses in these devices are pointed out. Thin film ohmic contacts to the devices call for careful attention. The role of an adhesion layer in multilayer metallization schemes is highlighted. In packaged devices, sites facing potential risks of delamination are indicated. As MEMS devices incorporate moving parts, there are additional issues due to adhesion of suspended structures to surfaces in the vicinity, both during chip fabrication and their subsequent operation. Proper surface treatments for preventing adhesion together with design considerations for overcoming stiction pave the way to reliable functioning of these devices. Adhesion–delamination issues in microelectronics and MEMS continue to pose significant challenges to both design and process engineers. This paper is an attempt to survey the adhesion characteristics of materials, their compatibilities and limitations and look at future research trends. In addition, it addresses some of the techniques for improved or reduced adhesion, as demanded by the situation. The paper encompasses fundamental aspects to contemporary applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

When two surfaces are drawn into intimate contact by physical and chemical forces, an adhesive union is formed accompanied by elastic/plastic deformation at the interface. An external pulling force is required to detach the two adherents. It is the magnitude of this pull-off force and the mechanisms of adhesion/decohesion that lay the groundwork of adhesion theory. Adhesion (defined as non-failure of the interfacial region under the service conditions) and delamination (loss of adhesion of a film from the substrate) have been pervasive problems hampering the performance of microelectronics and MEMS devices [1–8].

Different types of dissimilar material interfaces are encountered in contemporary microelectronic and MEMS structures (metal–metal, metal–ceramic, polymer–metal, polymer–ceramic, etc). Impairment of their functionality leads to safety and reliability concerns, making them major obstacles in achieving the full capabilities of devices [9–11]. Delamination has gained notoriety as a key triggering agent of mostly observed reliability problems in the microelectronics and MEMS industries. Figure 1 shows the initiation of crack and delamination in a two-layered structure.

Presently, there is scarce understanding of the phenomena governing adhesion, a shortfall that has seriously impeded science-based design and analysis, in particular as the devices

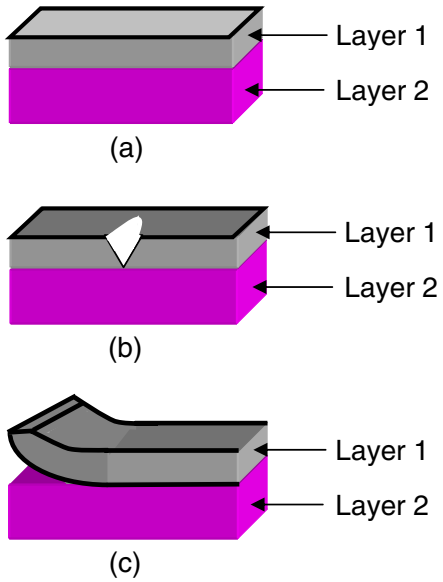

Figure 1. (*a*) Two-layered structure, (*b*) cohesive crack and (*c*) interface debonding or delamination.

are miniaturized, systems are integrated, and new materials and functions are introduced. Deeper understanding of adhesion phenomena will boost the development of new surface treatment processes.

Since silicon-based microelectromechanical systems (MEMS) are the integration of mechanical elements, sensors, actuators and microelectronics on a common Si substrate through the utilization of the micro-fabrication technology, a blended approach will be followed in this paper, treating microelectronics and MEMS issues jointly and shifting the focus to microelectronics or MEMS, as necessary. The paper is organized as follows: section 2 will differentiate between true and practical work of adhesion. In section 3, adhesional issues of thin films will be addressed. Thin film stresses will be dealt with in section 4. Properties of the adhesion layer of multilayer metallization used in semiconductor devices will be presented in section 5. Section 6 will treat adhesion problems in copper/low-κ interconnects. Section 7 will dwell upon surface preparation procedures for good adhesion. Section 8 will explain adhesion-related stiction phenomena in MEMS. In section 9, the role of adhesion in packaging will be described. Section 10 will make a retrospection of the topics covered in this paper and bring out the adhesion–delamination problems and their solutions followed by concluding remarks in section 11.

2. True (or fundamental) and practical (or technologically important) work of adhesion: the relevance of measurements

Broadly, adhesion is studied from two viewpoints. From the thermodynamic viewpoint, the *true work of adhesion* of the interface is defined as the amount of energy required for creating free surfaces from the bonded materials [12]:

$$W_{\mathrm{A}} = \gamma_{\mathrm{f}} + \gamma_{\mathrm{s}} - \gamma_{\mathrm{fs}}, \tag{1}$$

where γ_{f} and γ_{s} denote the specific surface energies of the film and the substrate, respectively, and γ_{fs} is the energy of the film–substrate interface. W_{A} is often determined by contact angle measurements. The true work of adhesion is a constant for a given film/substrate pair, e.g., for metals on ceramic, it is typically a small number $\sim$0.5–2 J m^{-2}.

Because a majority of adhesion test methods, notably, peel, stud-pull, scratch, blister, indentation and super layer delamination determine adhesion by delaminating thin films from the substrate, extraction of true adhesive energy from the total energy measurement is complicated [13]. The intricacy arises because the thin film and/or the substrate usually undergo plastic deformation during debonding from the substrate. Therefore, it is usually very difficult to measure fundamental adhesion for technologically important structures, due mainly to the inability to consider all energy dissipating processes during the test such as energy dissipation as heat in sonic emission, in fractoemission or locally in the deformation ahead of the crack front. Consequently, the measurement yields the *practical work of adhesion* or *interfacial toughness* [12]:

$$W_{\mathrm{A,P}} = W_{\mathrm{A}} + U_{\mathrm{f}} + U_{\mathrm{s}} + U_{\mathrm{fric}}, \tag{2}$$

where U_{f} and U_{s} are the energy expended in plastic deformation of the film and the substrate and U_{fric} is the energy loss due to friction. The discipline that enables quantitative solutions of crack propagation problems from stresses in different structures is called *linear elastic fracture mechanics* (LEFM) [14, 15].

It must be emphasized that fundamental adhesion is the energy required to break the bonds at the weakest plane in the adhering system under the measurement conditions used, whereas practical adhesion represents the energy required to disrupt the adhering system irrespective of the locus of failure [1]. Looking from a manufacturer's perspective, it is more relevant to improve the reliability of the structure being made by overcoming the interface problems instead of knowing the precise value of the fundamental adhesion.

3. Thin film adhesion

Microelectronics and MEMS devices extensively use thin films. The adhesion of these films is of paramount importance to the operation of the devices built by these films in contrast to macroscopic machines. Adhesion of a thin film depends considerably on the cleanliness of the surface upon which the film is deposited [13–17]. Optimum substrate roughness is necessary to ensure thin film adhesion. While a highly smooth substrate decreases adhesion tendency, a very rough substrate too is inappropriate from adhesion standpoint. It can result in coating defects, leading to thin film adhesion failures. It is always found that regardless of the deposition process employed, thin films always show an intrinsic stress, either tensile or compressive (figure 2), represented by negative and positive values, respectively. High residual stresses create adhesion problems, corrosion, cracking and deviations in electrical properties with respect to anticipated values. Thus, the proper deposition process is a prime necessity

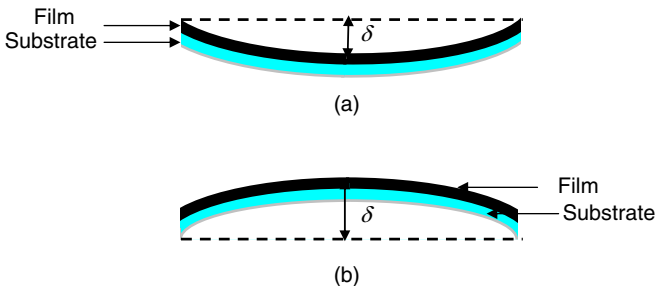

Figure 2. Stress in a thin film: (*a*) tensile and (*b*) compressive.

to minimize intrinsic stresses in thin films. Further, it must be noted that thin films exhibit comparatively more sensitivity to thermomechanical stresses than bulk materials. An incipient adherent coating lifts off after the device is subjected to thermomechanical stresses paralyzing device operation during use.

4. Stress-induced delamination of thin films

Residual stress in thin films comprises two main components: (i) thermal stress due to mismatching of coefficients of thermal expansion of film and substrate materials and (ii) intrinsic stress due to all other factors. Rapid deposition of films by evaporation or sputtering produces high-stress levels. If the film is not deposited at room temperature T_0, and if $T_{\text{deposition}}$ is the temperature of film preparation, E is Young's modulus, υ is Poisson's ratio of the film material, then assuming E and υ to be temperature independent, this stress is written as [18]

$$\sigma_{\text{th}} = \left\{\frac{E_{\text{film}}}{(1-\nu_{\text{film}})}\right\} \int_{T_0}^{T_{\text{deposition}}} (\alpha_{\text{film}} - \alpha_{\text{substrate}})\, \mathrm{d}T, \qquad (3)$$

where α_{film} and $\alpha_{\text{substrate}}$ are the coefficients of thermal expansion of the film and substrate, respectively. Likewise, chemical reactions, doping by diffusion or ion implantation, lattice mismatch, etc, are contributory factors to stress development [19, 20]. Table 1 displays typical values of elastic constants and thermal expansion coefficients of materials used in microelectronics/MEMS processing. These are representative values for illustrative and comparison purposes only; in practice, the values tend to vary over a broad range with the deposition parameters.

If large residual stresses introduced by deposition processes are not annealed out during device fabrication, they are subsequently relieved by delamination and fracture. Highly stressed films accumulate large amounts of strain energy. When the strain energy release rate exceeds the interfacial toughness of the film, delamination ensues [20]. The film may peel off from the surface; otherwise voids may be formed on temperature cycling. Compressive residual stresses cause film buckling and debonding, thereby forming open channels. An interface crack is driven by the stored elastic energy of the system, which is released by buckling. Buckling delamination is a multiscale phenomenon. It is induced by compressive stresses but moisture traces present at the film/substrate interface substantially lower thin film adhesion. This reduction in adhesion is predominantly due to a chemical reaction at the crack tip, which aids in rupturing of the bond. The crack velocity is strongly dependent on relative humidity for ceramics, bulk glasses and metal/SiO_2 interfaces. A noteworthy effect of water creeping to the interface results from lowering the surface energies of the newly formed surfaces at the crack tip. Smaller surface energies lead to a decrease in the true work of adhesion.

Stress is measured by determining the bow or warpage of the wafer before and after deposition. It is expressed as [18]

$$\sigma = \left(\frac{\delta}{t}\right)\left\{\frac{E}{(1-\nu)}\right\}\left(\frac{t_{\text{wafer}}^2}{3R^2}\right), \qquad (4)$$

where δ is the deflection of the centre of the wafer defined as the difference in height between the centre and the edge, t is the film thickness, t_{wafer} is the thickness of the wafer and R is the radius of the wafer.

Silicon dioxide is naturally compressively strained on silicon. This is the reason why scanty MEMS devices with freestanding silicon dioxide have been reported in the literature. Polysilicon films are made of both compressive and tensile strains, depending on the deposition parameters. The IC industry has invariably used compressive polysilicon, while MEMS researchers have developed processes for controlling stress in polySi. Silicon nitride films are highly tensile stressed on silicon. However, the stress rapidly declines and is even altered into compressive stress by incorporating more silicon than prescribed by the formula for stoichiometric silicon nitride. Stress gradients cause cantilever bending. Figure 3 shows the effect of stress on a cantilever beam.

Stress-controlling parameters in polysilicon and silicon nitride film preparations are given in the following investigations:

(i) In one study [21], *normal polysilicon* (stress = 292 MPa, deposition rate = 100 nm min^{-1}) was deposited at 630 °C, 250 mTorr pressure, SiH_4 flow back = 35 sccm, SiH_4 flow front = 115 sccm. *Low-stress polysilicon* (stress = 14 MPa, deposition rate = 37.7 nm min^{-1}) was deposited at 590 °C, 250 mTorr pressure, SiH_4 flow back = 90 sccm, SiH_4 flow front = 80 sccm. Reference [22] also presents optimized parameters for polysilicon deposition.

(ii) Increasing the silicon component of the films alters the intrinsic residual stress in Si_3N_4 films. The intrinsic residual stress of Si-rich Si_xN_y films is lower than standard Si_3N_4 due to volumetric distortion of the Si–Si_xN_{4-x} tetrahedral unit brought about by a reduction in the local atomic strain of Si–N bonds. The residual stress in Si_xN_y films decreases with increasing partial pressure of Si containing reactant (typically SiH_4, SiH_2Cl_2, etc). Since the index of refraction increases with increasing Si content, the residual stress is inversely proportional to the index of refraction. The stress may be varied from tensile compressive in the transition from stoichiometric Si_3N_4 to Si-rich low-stress nitride. Following deposition, mechanical stress in Si_xN_y remains due to (a) the mismatch between the coefficients of thermal expansion

Table 1. Properties of materials used in microelectronics and MEMS [18].

Sl. No.	Material	Young's modulus (GPa)	Poisson's ratio	Coefficient of thermal expansion (10^{-6} K^{-1})
1.	Si (single-crystal)	190	0.26	2.3
2.	PolySi	161	0.23	2–2.8
3.	SiO_2	57–69	0.17	0.7
4.	Si_3N_4	314	0.33	3
5.	Al	69	0.33	22.8
6.	Cu	117	0.33–0.36	17.1
7.	Au	75	0.42	14.2
8.	Eutectic solder (Sn-37Pb)	30.2	0.4	24
9.	Underfill	6	0.35	30
10.	Polyimide PMDA/BPDA/TFMOB	7.5 (in-plane) 8.0–15.0 (out-of-plane)	0.35 (in-plane)	6.0

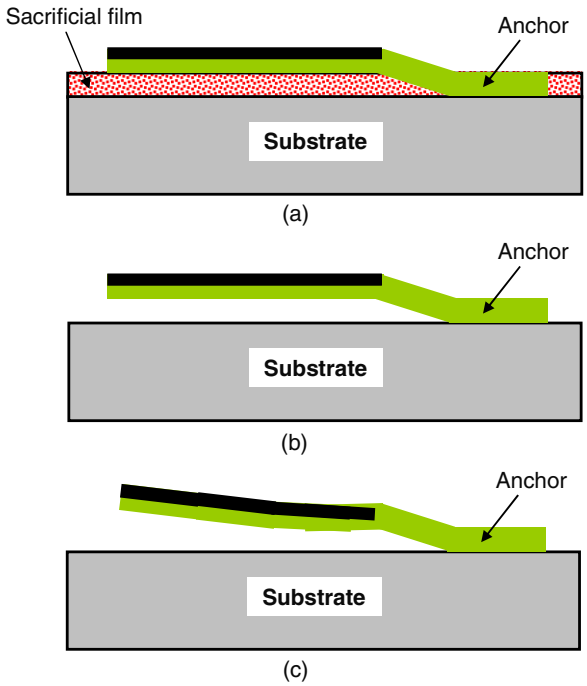

Figure 3. Stress gradient in cantilever: (*a*) before release, (*b*) after release and (*c*) after bending.

of the Si substrate and the film and (b) intrinsic stresses within the film. The thermal component of this stress is a small, compressive stress while the intrinsic component is a much larger tensile stress.

Olson [23] generated low-pressure chemical vapour deposition (LPCVD) silicon nitride films with an index of refraction ranging from about 2.04 to 2.82 and residual stress ranging from about 700 MPa tensile to −90 MPa compressive. The relationship between residual stress and index of refraction was characterized and results compared with those presented in the technical literature. Increase in the index of refraction beyond about 2.3 by means of increasing the gas flow did not reduce the residual stress appreciably but had a significant detrimental impact on the thickness uniformity and deposition rate. In contrast to results reported by other researchers, uniformity was not observed to increase with increasing dichlorosilane (DCS)/NH_3 ratio in this study. Ultra-low-stress nitride was deposited at DCS/NH_3 ratios of 4 : 1 and higher temperatures than traditionally utilized for Si_3N_4 deposition. Residual stress of $\sim 0 \pm 10$ MPa was achieved at index of refraction of 2.25.

Conventionally, low-stress plasma-enhanced chemical vapour deposition (PECVD) SiN_x is commonly produced by mix frequency mode, which alternatively applies the HF (13.56 MHz) and LF mode. However, due to the low deposition rate of LF mode, the combined deposition rate of mix frequency mode is low for depositing homogenous SiN_x layers. Ciprian *et al* [24] used a high power up to 600 W to produce low residual stress (0–20 MPa) films with higher deposition rate (250–350 nm min^{-1}). The higher power not only led to higher dissociation rates of gases which resulted in higher deposition rates but also brought higher N bonding in the SiN_x films and higher compressive stress from higher volume expansion of SiN films, which compensated the tensile stress and produced low residual stress.

Stresses are built up in IC layer stacks during the backend processes, namely, metal depositions, edging and chemical vapour deposition, etc. During packaging processes such as die attach and moulding; testing procedures, such as temperature cycling and moisture assessment and/or actual service, thermally induced deformations and stresses further propagate in the IC layers and the surrounding packaging materials. If these deformations and stresses aggravate, they become critical for product assembly. This happens because they influence the solder mount attachment, which provides the solitary electrical/mechanical connection of the electronic component to the printed circuit board. In the worst-case scenario, the developed deformations and stresses may ultimately jeopardize the targeted lifetime of the product.

5. Adhesion of metal films and need of multilayer metallization schemes

Metallization of semiconductor wafers is a multifunctional requirement that is fulfilled by the multilayer thin film technology (figure 4) [25–34]. The high diffusivity of silicon through silicide layers is problematic in silicon–silicide–metal systems because heat treatment causes excessive interdiffusion

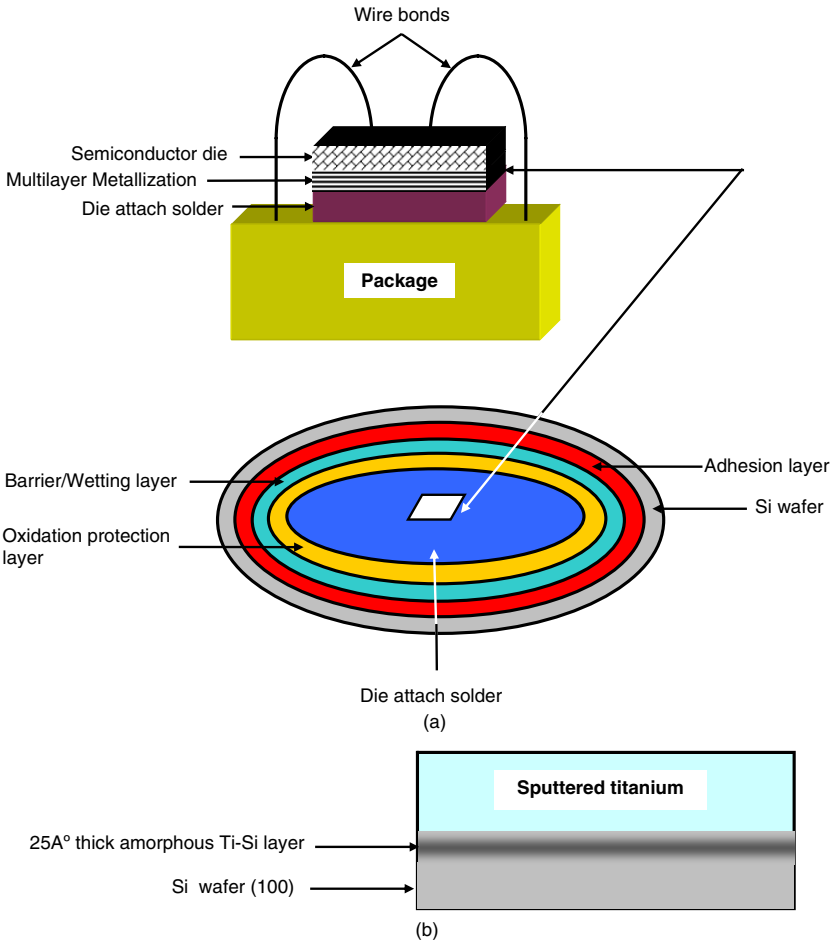

Figure 4. (*a*) Semiconductor die mounted on package and wire bonded; multilayer backside metallization scheme is shown. (*b*) Diagrammatic representation of Ti–Si intermixed interface structure for Ti sputtering on Si.

between the metal and the silicon through the silicide layer. For backside metallization, the multilayer system generally consists of an *adhesion layer* such as Ti, Cr; a *conduction layer* (copper in some cases); a *barrier/solder wetting layer* such as Ni, Pd, Pt and Co.; an *oxidation protection layer* such as Au and Pt and a *die attach solder*, e.g., AuSn, PbSn, etc. For front side metallization, there are schemes such as Cr–Au and Ti–TiN–Pt–Au with wire bonds.

Ti and Cr layers serve as glue materials. These are required because the best electrical conductors (silver, copper, gold) do not stick to SiO_2 albeit adhering well to silicon. Silver, copper and gold do not stick to SiO_2 but instead tend to ball up during a heat treatment even when the temperature never reaches the melting point of the metal (figure 5) [27].

Adhesion of a film to its substrate requires a physical interlocking, interdiffusion of the films or a chemical bonding between film and substrate in order to be effective. In Ti–Si system, an intimately intermixed 25 Å thick amorphous Ti–Si is formed at the interface. Bonding of Ti to Si surface is favoured by its large (negative) enthalpy of formation: 2 a-Si + Ti $\rightarrow$ a-TiSi + a-Si, $\Delta H_f = -62\,\mathrm{kJ\,mol^{-1}}$. Also, titanium has a negative heat of reaction with SiO_2 and breaks down SiO_2 to form titanium oxide. Systematic experiments have established this and have demonstrated that only the most reactive of the transition metals (e.g. titanium, zirconium, hafnium, vanadium, niobium) are expected to adhere to SiO_2 on this basis. Early transition metals adhere strongly to SiO_2 because they dissociate the substrate and form a strong mechanical bond during a thermal treatment in which external oxygen sources are absent, e.g. high vacuum environment.

Both Ti and Cr show high reactivity as manifested by the formation of their oxides, nitrides or carbides. Their diffusion through the Au layer is immediately followed by oxidation as a surface species. Ti forms brittle intermetallic phases such as $TiAu_2$, TiAu and Ti_3Au [31]. The oxidation of Ti degrades the solderability/wire bondability, thereby lowering the bonding adhesion. This is prevented by introducing Pt as a barrier metal. Ti diffuses to Pt through grain boundaries. Incorporation of a thin layer of TiN between Ti and Pt inhibits the formation of TiPt intermetallics.

For achieving good adhesion, platinum metallization on a polished sapphire substrate requires a thin <20 nm buffer layer such as Ti or Zr. Benhardt *et al* [29] found using AES, SIMS, XRD and wire bond tests that Zr exhibited performance superior to that of Ti. While at 200–700 °C-operating temperatures there was significant migration of Ti through Pt film, Zr was relatively less mobile. Further, Pt/Zr/sapphire structure suppressed the delamination failure of wire bonds to the device.

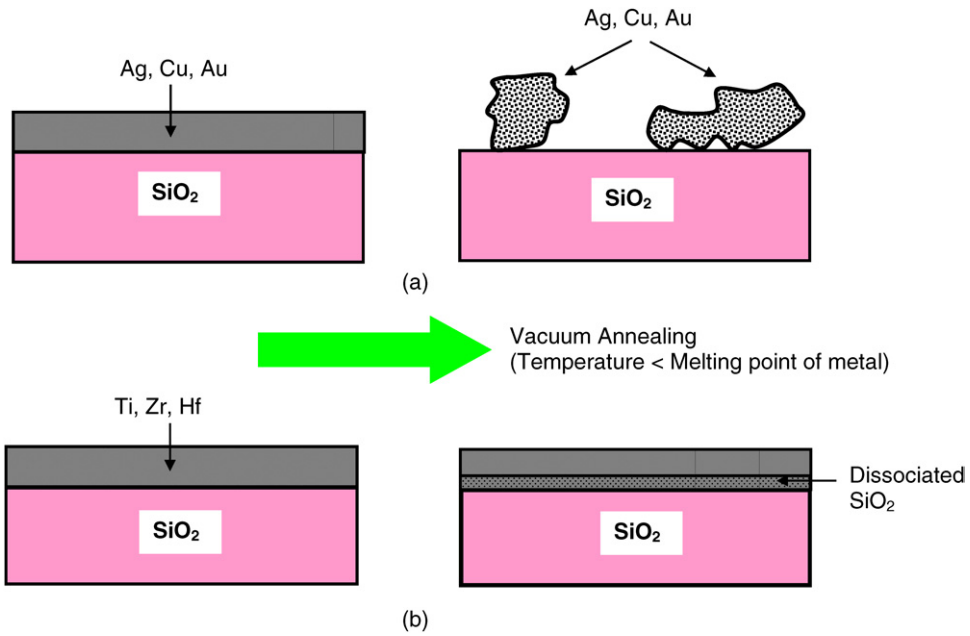

Figure 5. Behaviour of (*a*) good electrical conductors and (*b*) reactive transition metals towards SiO_2.

Given below are illustrative examples where different researchers have skillfully addressed stress build-up issues and obtained solutions for stress-induced delamination:

(i) Generally, a low-stress film is more durable than a high-stress film because of its fewer cracks and wrinkles. Chu *et al* [35] determined the effect of Al film sputtering power for deposition on a Corning EAGLE 2000 glass substrate. The stress of the Al film was found to change from tensile to compressive with increasing sputtering power. It was +460.7 MPa at 100 W dc power and −1438.5 MPa at 800 W. From the viewpoint of minimal Al film stress, the sputtering power of the Al film ranging from 200 to 400 W was optimal.

(ii) Waters [36] carried out stress analysis and mechanical characterization of tungsten thin films. A dc magnetron sputter system was used to deposit tungsten films, with film thickness and residual stress uniformity being of primary interest. Residual stress measurements of the tungsten films were made using a wafer curvature technique and x-ray diffraction. The results of the two techniques were compared and found to be within 20%. Ar pressure was found to influence the thin film residual stress with lower Ar pressures leading to compressive residual stress (−1.5 GPa) and higher Ar pressures producing tensile residual stress (1 GPa). Thus, thin film residual stress was controllable through Ar pressure.

(iii) Jeon *et al* [37] fabricated Pt electrodes on Si substrates by dc magnetron sputtering using two kinds of diffusion barriers: ZrO_2 (1500 Å)/SiO_2 (6000 Å) and SiO_2 (6000 Å), figure 6. The intent was to deposit PZT films of thickness greater than 10 μm for microsensor and actuator applications. They measured the residual stresses of these composite films by x-ray diffractometer, and found that Pt/ZrO_2/SiO_2 buffer system had a smaller tensile stress than the Pt/SiO_2 so that the 30 μm thick PZT film could be deposited on ZrO_2/SiO_2 by screen printing without peeling off. ZrO_2 played the role of an adhesion layer like titanium film because the coefficient of thermal expansion of ZrO_2 ($5 \times 10^{-6}\,^{\circ}C^{-1}$) had an intermediate value between that of Si ($4.5 \times 10^{-7}\,^{\circ}C^{-1}$) and Pt ($8.85 \times 10^{-6}\,^{\circ}C^{-1}$). Therefore, for this problem, ZrO_2/SiO_2/Si multilayer structure was obviously a better solution than SiO_2/Si multilayer.

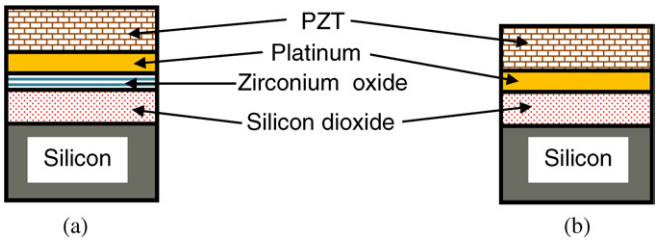

Figure 6. Multilayer stacks: (*a*) PZT/Pt/ZrO_2/SiO_2/Si and (*b*) PZT/Pt/SiO_2/Si.

(iv) Several solutions have been practiced to promote the adhesion of copper [38, 39] such as a multilayer diffusion barrier comprising (i) a refractory metal such as tungsten (W), titanium (Ti), tantalum (Ta), molybdenum (Mo), and a refractory metal nitride e.g. WN_x, TiN, TaN; and a second sublayer formed from a refractory metal nitride, and a refractory metal silicon nitride such as $TiSi_xN_y$, $TaSi_xN_y$, WSi_xN_y; (ii) a very thin multilayer diffusion barrier composed of even thinner sub-layers, where the sub-layers are only a few atoms thick; (iii) a hybrid type nanocomposite diffusion barrier formed by atomic layer deposition using precursors composed of a Ti precursor and a Ta precursor.

(v) Microelectronic devices do not generally utilize blanket thin films, but instead utilize intricate wiring interconnections where metal lines have lateral dimensions

comparable to their thickness. The lines are typically sheathed with a thin (<100 nm) elastic diffusion barrier layer and supported mechanically by flanking dielectric materials. Traditional dielectric materials are SiO_2 glasses, which are brittle and show elastic behaviour. However, several new classes of organic materials, including spin-on polymers, have been developed to replace SiO_2. These polymers behave in a ductile fashion, allowing plastic energy dissipation during debonding akin to metal layers.

Litteken and Dauskardt [32] examined the adhesion or interface fracture resistance of structures containing arrays of polymer lines with varying aspect ratio. Macroscopic adhesion values were determined by evaluating the critical strain energy release rate, G_c, for debonding of the patterned interface. The yield properties of the polymer films as a function of film thickness were also investigated.

Decreasing aspect ratio of the polymer lines was found to drastically increase the interface fracture energy. Adhesion values were augmented by more than 50% for lines with the smallest aspect ratio compared with the large aspect ratio lines that were wide with respect to their thickness. The increase in adhesion was associated with growing contributions from plastic energy dissipation in the patterned lines. Due to falling lateral constraint of the lines with diminishing line width, the stress state in the polymer line became progressively less triaxial. Consequently, the polymer yielded more readily as the stress state altered from plane strain, in the case of broad lines or the blanket film, to one of plane stress for the slender lines. The observed fracture resistance behaviour was strikingly similar to the changeover from plane strain to plane stress fracture frequently noticed in bulk metals and polymers. These results undoubtedly supported the proposition that macroscopic adhesion values of interfaces in interconnect structures were severely influenced by the geometry and size of ductile features neighbouring the interface of interest. These inferences provide valuable inputs to device designer that ought to be taken into consideration at the time of pattern layout to overcome such adhesional problems.

6. Copper metallization and backend-of-line (BEOL) interlayer dielectrics

With shrinkage of circuit geometries, the intrinsic circuit delay (RC) increases. The unified influence of higher resistance (R) in the metal interconnects, and also capacitance (C) effects from the interconnects are responsible for the delay rise [40]. Strategies to mitigate these parasitic effects include utilization of metals with lower resistivity and higher electromigration resistance values, and provision of electrical isolation with insulating materials having low dielectric constants (figure 7) [40–43]. Copper has removed and replaced the aluminium alloy AlSiCu as the new favourite interconnect metal, compelling also the introduction of damascene processing. Alternative materials for SiO_2 with a lower dielectric constant are being developed and are seeking entry into the mainstream processing. Moreover, in an effort to lower the dielectric constant even more, these materials are being made increasingly porous.

The integration and introduction of the aforesaid low-κ materials is a main bottleneck due to the inferior thermal and mechanical integrity of these materials and the inherited feeble interfacial adhesion. In particular the forces resulting from packaging-related processes such as dicing, wire bonding, bumping and moulding are critical. These forces easily cause cracking, delamination and chipping of the IC backend structure if corrective measures are not taken. Because copper can hardly be removed by wet/dry etching, the chemical-mechanical polishing (CMP) technique is used to remove the excess copper layer in the damascene structure. As a result, the delamination failure modes at the dielectric layers are often observed when applying the mechanical/thermal loadings on to this advanced Cu/low-κ IC and its succeeding packaging processes. Increasing the applied pressure, friction coefficient and the copper thickness induces the possibility of failure of the low-κ layer. However, reduction in the applied pressure and coefficient of friction decreases the throughput speed in the fabrication. Accordingly, a thin copper layer is preferred to prevent the possibility of the failure of the low-κ material; the same is controlled by the copper deposition process.

For a stack of blanket films, there is no driving force for delamination. The reason is that interfacial stress is negligible. No energy is released as the interfacial defect size changes. However, when a blanket film covers a patterned film [33, 34], the energy release rate of channel cracking is increased appreciably by the underlying copper pattern. When a patterned underlayer exists, the thermal mismatching between the materials produces an interfacial stress providing the driving force for delamination. This driving force for delamination is strongly dependent on the pattern underneath

Doping of silica-based dielectrics with carbon atoms and other organic molecules is carried out to reduce the permittivity of backend-of-line (BEOL) interlayer dielectrics. The resulting organosilicate glass (OSG) has a relative permittivity value <3.0. It has approximately half the density of fused silica. The open network structure makes the diffusion and absorption of reactive molecules into the OSG much easier. The four-point-bend and double-cantilever beam techniques have been used [44–49] to demonstrate that the cohesive and adhesive fracture of OSG strongly depends on the chemical reactivity of the testing environment, as revealed by pH or relative humidity (% R.H.) measurements. Tsui *et al* [50] showed that the quantity of absorbed reactant in the organosilicate glass films was controlled by exposing the capped organosilicate films to aqueous solutions for various periods of time. They asserted that the initial degradation of the critical adhesion energy of the interfaces between OSG and tantalum, tantalum nitride (TaN_x), silicon nitride (SiN_x) and silicon dioxide (SiO_2) capping layers was very fast, but that the same was fully recoverable to the 'dry' value by baking the samples. They proposed a quantitative model based on Henry's law for predicting the adhesion degradation rate as a function of exposure time to water vapour.

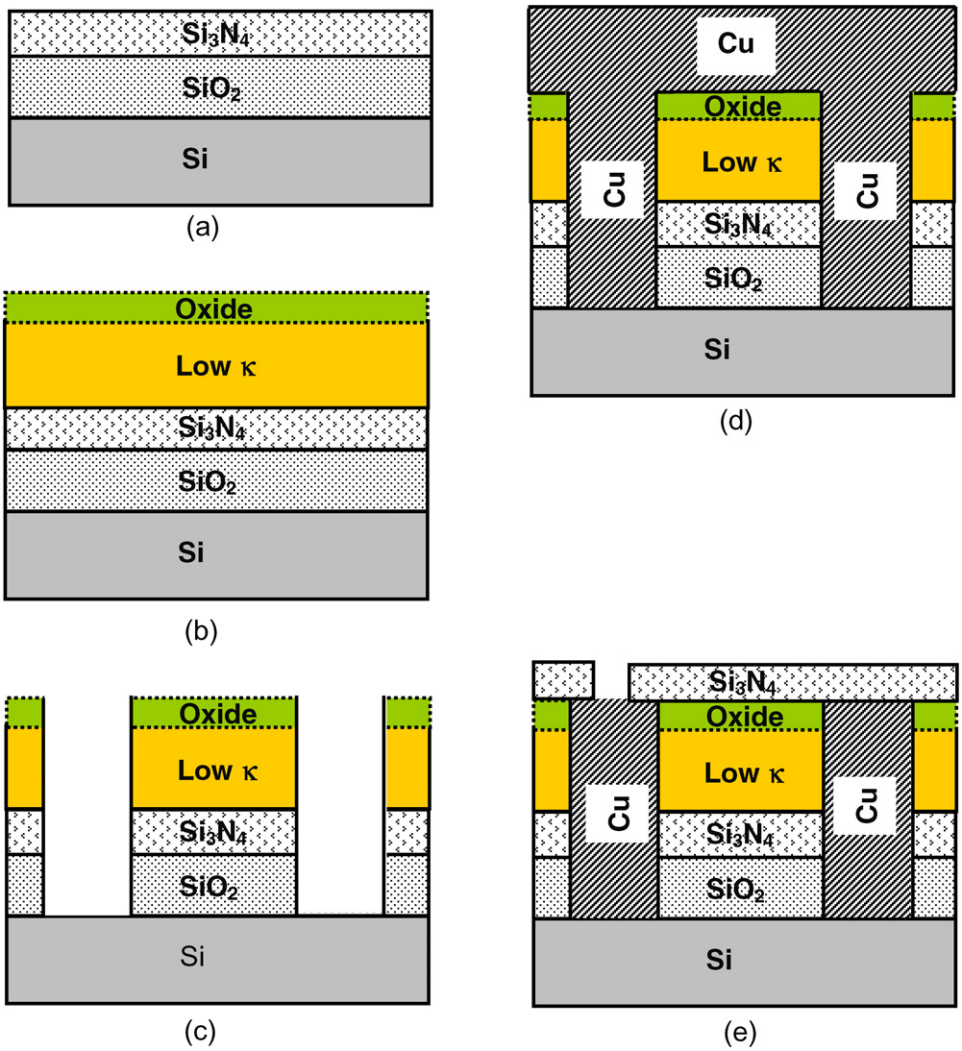

Figure 7. Cu Damascene /low κ dielectric process: (*a*) Starting structure, (*b*) deposition of low κ dielectric and capping oxide, (*c*) patterning and etching low κ dielectric, (*d*) Cu deposition and annealing, (*e*) chemical mechanical polishing of Cu and capping nitride deposition.

7. Surface cleanliness and preparations for improving adhesion

Numerous apparently dissimilar adhesion problems have a common root cause. They arise primarily from one variable: *surface cleanliness*. Semiconductor surface must be free of oxide for ensuring strong metal adhesion. This is accomplished through chemical etching by HF and by argon sputtering.

Surface preparation through surface activation and contamination removal by *plasma processing* is finding widespread usage in industry [17]. *Surface contamination removal* by plasma is achieved by an ablation process involving physical sputtering and chemical etching as the main tools. Organic contaminants such as residual solvents, epoxy residues, oxidation and mould release compounds undergo repetitive chain scission under the bombardment by plasma. This progresses until their molecular weight is adequately low to enable volatilization.

Surface activation is a process where surface functional groups are replaced with different atoms or chemical groups from the plasma containing ions, electrons, free radicals and other neutral species when plasma source gases such as argon, oxygen, hydrogen, or a mixture of these gases are employed.

Plasma processing removes the contaminants and makes the surface clean and active resulting in improved wire bonding and decreased possibility of delamination at the interfaces [17].

8. Auto-adhesion or stiction in MEMS

Inclusion of moving parts is a distinguishing characteristic of MEMS. Because MEMS devices respond to mechanical signals, they use structural topologies that require physical motion, e.g., suspended plates, cantilever beams, diaphragms or membranes, etc. These microstructures have relatively large areas but a very small stiffness. Also, they are fabricated at separation distances of only a few micrometres from their supporting substrates. These constructional features make MEMS devices highly prone to surface forces, causing the suspended members to deflect towards the substrate.

Adhesion-spurred failures occur in MEMS when suspended elastic members surprisingly fasten to their

substrates. In these conditions, the elastic member collapses and permanently adheres to the underlying substrate. Because the actuation forces generated artificially on a micro-scale are very miniscule, it is frequently not possible to separate these surfaces again for restoring normal device functioning. This generally brings the mobile part in MEMS device to a halt. Such a type of irreversible device failure is a dominant source of yield degradation in MEMS. It requires the occurrence of two different phenomena. Firstly, the device must be subject to a force sufficiently strong to collapse the elastic member, thus pulling it in contact with the substrate. Secondly, after contact of the elastic member is established and the force is withdrawn, the intersolid adhesion must supersede the elastic member restoring force, thereby keeping the device permanently pinned to the substrate. Both these situations appear during the device fabrication (such as exposing the suspended member to an aqueous rinse and dry cycle) as well as in its routine operation (e.g., by pulling down by electrostatic forces and collapse by acceleration forces). The adhesion of contacting surfaces under the action of surface forces is termed *auto-adhesion* or *stiction* (a subtraction of 'static friction') [51–72].

8.1. Surface and interfacial forces in stiction

Important surface forces include capillary condensation, molecular van der Waals forces, electrostatic forces, hydrogen bridging and solid bridging [53, 64, 65]. These surface forces are much more pronounced in MEMS than they are in the macroscopic world because of the large surface-to-volume ratios in microsystems. Hence they play crucial deterministic roles in MEMS.

Considering a liquid layer between two solid plates, if the contact angle θ_C between liquid and solid is less than 90°, the pressure inside the liquid drop is lower than outside, and a net attractive force exists between the plates (figure 8(*a*)) [53]. This force originating from surface tension of the liquid–air interface and serving as an adhesive between the plates is called the *capillary force*. The surface interaction energy is given by [64]

$$e_{\text{cap}} = 2\gamma_{\text{la}} \cos\theta_C|_{z\leqslant d_{\text{cap}}}, \qquad e_{\text{cap}} = 0|_{z>d_{\text{cap}}}, \tag{5}$$

where γ_{la} is the surface tension of the liquid–air interface and z is the gap between the plates. *Capillary condensation* of water vapour will occur if the distance between two flat plates is smaller than a characteristic distance of capillary condensation, $z = d_{\text{cap}}$ [64]:

$$d_{\text{cap}} = \frac{2\gamma_{\text{la}}\upsilon\cos\theta}{RT\,\log(\text{Relative Humidity})}, \tag{6}$$

where υ is the molar volume of the liquid, θ is the contact angle of water on the surface, R is the universal gas constant and T is the absolute temperature.

If the solid–air surface tension is smaller than the sum of the liquid–air and solid–liquid surface tensions, the liquid will be non-spreading (figure 8(*b*)) [53]. When the solid–air surface tension is larger than the sum of the liquid–air and solid–liquid surface tensions, spreading of the liquid is energetically

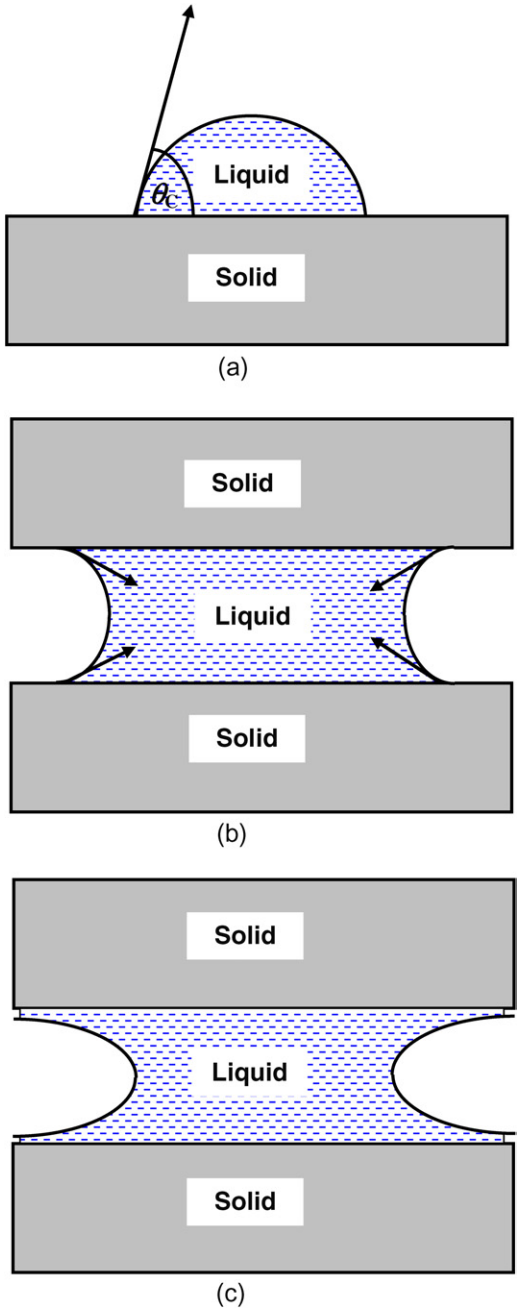

Figure 8. (*a*) Liquid drop on a solid; θ_C is the contact angle. (*b*) and (*c*) Liquid bridging two solid plates showing non-spreading and spreading liquid cases, respectively.

favoured. Then a drop bridging two surfaces will form thin liquid films outside the bridged area (figure 8(*c*)) [53].

van der Waals forces are produced by mutual electrical interaction of induced dipoles in the two plates. The surface interaction energy due to van der Waal's forces is given by [64]

$$e_{\text{vdW}} = 0|_{z>d_{\text{ret}}}, \qquad e_{\text{vdW}} = \left\{\frac{A_{\text{Ham}}}{(24\pi z^2)}\right\}\Bigg|_{d_{\text{co}}<z<d_{\text{ret}}}, \tag{7}$$

$$e_{\text{vdW}} = 0|_{z<d_{\text{co}}},$$

where A_{Ham} is the Hamaker constant of the molecule and z, again, is the distance between the surfaces. d_{ret} is the

distance of the 'retarded regime', further than 20 nm away. On coming closer, the attractive van der Waals force changes into a repulsive one (electron shell deformation), and a universally used cut-off distance is $d_{co} = 0.165$ nm, whose value is slightly less than the inter-atomic distance. The Hamaker constant of most non-polar molecules lies in the range of $(0.4–4) \times 10^{-19}$ J.

Casimir force [65] has been associated with van der Waals forces. The following comparisons have been made: (i) *van der Waals force* is concerned with approximation of perturbation theory applied to electrostatic interaction of two dipoles. This is valid only when the separation $z < d_{ret}$, with d_{ret} being the retardation length, and corresponding to the transition between the ground and the excited states of the atom. The attraction is proportional to $1/z^3$ and is affected by material properties. (ii) *Casimir force*: when the separation $z \sim d_{ret}$ or $z > d_{ret}$, retardation effects come into play. The attraction is proportional to $1/z^4$ and is not influenced by the properties of the material. Thus the Casimir forces contribute at longer distances than the van der Waals forces.

Electrostatic forces across the interface arise from a difference of work functions or charging of opposed surfaces, e.g., tribocharging of rubbing surfaces and ion trapping in oxide layers. *Hydrogen bridging* occurs due to the formation of hydrogen bonds between hydrogen and oxygen atoms of adsorbed water layers on hydrophilic silicon surfaces.

The Coulomb interaction between charged surfaces will give rise to a force written as [64]

$$F = \frac{\varepsilon V^2}{2z^2}, \tag{8}$$

where ε is the dielectric permittivity of the material in the gap and V is the voltage difference between the plates. The surface interaction energy is [64]

$$e_{EL}(z) = \frac{\varepsilon_o V^2}{2z}. \tag{9}$$

When MEMS surfaces are covered with OH bonds, H-bridging raises the surface interaction energy. Because H-bridging is a short-range force (a conventional OH$\cdots$O bond is 0.27 nm), it is more sensitive to surface roughness as compared with capillary condensation.

8.2. Pinning by contact adhesion: adhesion or detachment length

Intersolid adhesion due to the change in the energy stored at the contact area with respect to the elastic member deformation often surpasses the restoring force of the member. In real surfaces, the magnitude of the adhesion energy is decided by the nature of the interface. Consider the peeling of an elastic cantilever beam of length l, width w, thickness t, height h and Young's modulus E, from an adhesive surface (figure 9). The beam is sticking to its substrate at a distance $d = l - s$ from its tip. The accumulated elastic energy of the beam in the segment $0 \leqslant x \leqslant s$ induces a restoring force tending to peel the beam from the substrate. The energy of adhesion stored in the part

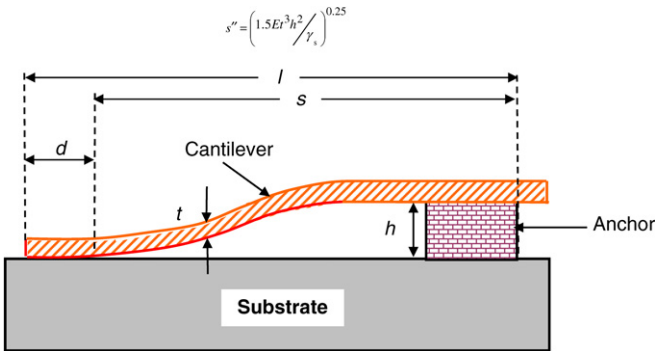

Figure 9. Schematic diagram of a cantilever beam adhering to the substrate.

$0 \leqslant x \leqslant l$ induces another force that attaches the beam to the substrate. The equilibrium peel distance s'' is determined by the counterbalancing of these two energies. At equilibrium, s'' minimizes the total energy of the system, i.e. the sum of bending and adhesion energies. It is expressed as [55]

$$s'' = \left(\frac{1.5Et^3h^2}{\gamma_s}\right)^{0.25}, \tag{10}$$

where γ_s is the surface energy per unit area of the bond. If $s'' < l$, the energy curve has a single equilibrium point and if $s'' > l$. there is no equilibrium point. Thus if $s'' < l$, the beam is pinned to the substrate, and if $s'' > l$, it is free. The critical length of cantilever beam is smaller than the detachment length s'' because prior to complete detachment, shear deformation will take place at the tip and the beam will touch the substrate subtending an angle. Ignoring the residual stress and the stiffening due to stretching, the formulae for critical length of doubly clamped beams and the critical radius of circular membranes show the same dependence on t, h, E and γ_s.

8.3. Adhesion by electrostatic pull-down

Tip deflection as a function of the applied voltage U is obtained from the balance between the electrostatic pull-down and the restoring elastic forces. The system becomes unstable (pull-in) if the pull-down force increases faster than the restoring elastic force with increasing $y(x)$, the deflection at position x along the cantilever. A general expression for the pull-in voltage of cantilever, doubly clamped beam and membrane is [53]

$$U_{pi} = \sqrt{\frac{cEh^3t^3}{\varepsilon l^4}}, \tag{11}$$

where ε is the permittivity and l represents the total length in the case of cantilever and doubly clamped beams, and the radius in the case of a circular membrane. Numerical constant $c = 0.28$, 11.9 and 2.27 for cantilever, doubly clamped beam and clamped circular membrane, respectively [53].

8.4. Anti-stiction measures

Pinning is a two-step process, namely, mechanical collapsing and adhesion to the substrate, either of which is prevented if

the stiffness of the microstructure is sufficiently high. The absence of liquid phase eliminates the capillary force. In the *freeze-drying* method [55], this is done by freezing of the solution and its subsequent sublimation but the volume change of rinse solution creates a damaging stress for the structure.

In several rinse procedures, the etchant is replaced by *p*-dichlorbenzene, which is a liquid at 70 °C. At room temperature, the solidified dichlorbenzene is easily sublimated in a vacuum chamber [54].

In *supercritical drying*, the rinsing solution is slowly replaced by liquid CO_2 at elevated pressure inside a chamber, and the sample is taken to the critical point of CO_2 at ∼72 atm where the liquid–gas interface is non-existent.

After rinsing with DI water, the HF is gradually replaced by organic solvents and finally by photoresist. After hardening the resist, it is dry removed in an O_2 plasma.

Dry etching of sacrificial layers is done by HF in vapour phase at a high temperature. As this attacks the silicon nitride layer, weaker sacrificial layers like plastics are convenient because they are etched by undamaging O_2 plasma or ozone [56].

The *liquid-bridge cleavage* method utilizes a sharp corner patterned near the weakest point in the structure to split the liquid bridge into two droplets that tend to reside near the anchors where the effect of capillary force is minimal.

To obtain a higher contact angle, preferably obtuse angle, hydrophobic *self-assembled monolayer (SAM) coatings* are made by silanization of silicon surfaces with organic groups by surface treatment with OTS (octadecyltrichlorosilane) precursor molecule. It involves substitution of the water rinsing by an organic solvent in a sequence of dilution steps, followed by SAM growth and replacement of water solvent in a reverse series of dilutions. The high contact angle ∼114° achieved by this process enables recession of water from the surfaces leaving them in dry state.

Intersolid adhesion is reduced if the contact area between the elastic member and the substrate is decreased. In practice, this is accomplished by texturing the contact surface. The texturing is deliberately introduced by constructing a periodic array of small supports commonly referred to as 'dimples'. These supports are constructed by etching small indentations into the sacrificial layer. This is done before the deposition of the suspended member, causing the formation of protrusions in the structural layer.

The deposition of water-repellent flourocarbon (FC) layers on the surfaces of the structures is helpful in avoiding the post-release sticking of the mechanical structures; such layers are formed in plasma reactors when operated with CF_4 and H_2 or CHF_3. With FC bumps, a freestanding membrane, (300 μm × 300 μm) in size, could be touched to the substrate more than 10 times without sticking.

Electrostatic pull-in to the substrate is avoided by electrical shielding in order to give the substrate locally the same potential as the structures directly above.

9. Adhesion issues in microelectronics/MEMS packaging

9.1. Wire bond packages

The *plastic quad flat package* is a leadframe-based plastic encapsulated enclosure, representing a mainstay package for the ASIC industry (figures 10 and 11). Interfacial delaminations on the die top, around the ball bond or wedge bond, between die, die attach and die pad, inside the substrate have detrimental effects on heat dissipation. Delaminations at critical locations constitute the foremost criteria of package reliability in industry standards and customer liability guidelines.

Different types of failure modes, such as cracking (passivation, package body, etc) and/or metal fatigue (wires, solder connections, etc) control the reliability of microelectronic packages [73–90]. Both these failures take place either on the *first level interconnections*, which are the interfaces within an IC package, or on the *second level interconnections*, which are the interfaces amidst the IC package and the printed circuit board (PCB) [3]. Interfacial delamination has a strong tendency of occurrence inside an IC package because of the large differences in coefficients of thermal expansions. Interfacial stresses occur between every two neighbouring layers of materials during the manufacturing process, its testing and finally its application. Due to the large differences in the thermal–mechanical properties, some of the stresses are appreciably high so that the material failures inevitably take place at sites of high stresses, particularly adjoining the interfaces. Alternatively, the stresses are so high that microcracks are initiated somewhere near an interface, while the global structure (the IC assembly) remains unharmed. Due to the temporal dependence of the material properties, such microcracks undergo further propagation during processing and application, and hence reduce the reliability. Because of the nature of a multilayer structure composed of different materials, multiple sites of potential interfacial delamination act competitively with each other in an assembly. First level interface delamination, in particular its initiation, is strongly aggravated by the moisture distribution in the IC package. Second level type of failure occurs at the solder joints having smaller load carrying areas, implying higher stresses in the solder connections. Hence, microcracks tend to initiate and propagate fast through the smaller connection areas.

Zhao and Pang [80] carried out a comprehensive investigation of delamination control in a plastic package. As a general analysis methodology, the improvement of delamination performance is reduction in the real value of the defined evaluation index X such as stress, strain and deformation, or enhancement of the critical value X_C of the corresponding index, which is described as [80]

$$X \leqslant X_C. \tag{12}$$

To cite an example, the tensile stress of an interface is 57 MPa (X) under working load and the adhesion tensile strength of the bi-material interface is 52 MPa (X_C). So the delamination

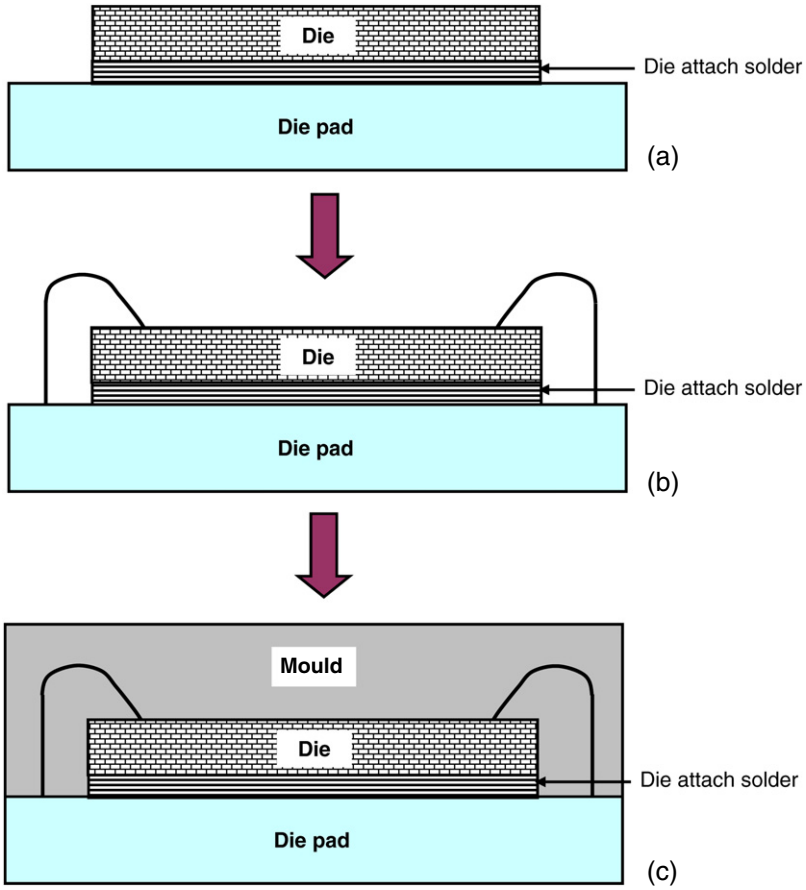

Figure 10. Wire bond packaging: (*a*) die attachment, (*b*) wire bonding and (*c*) moulding.

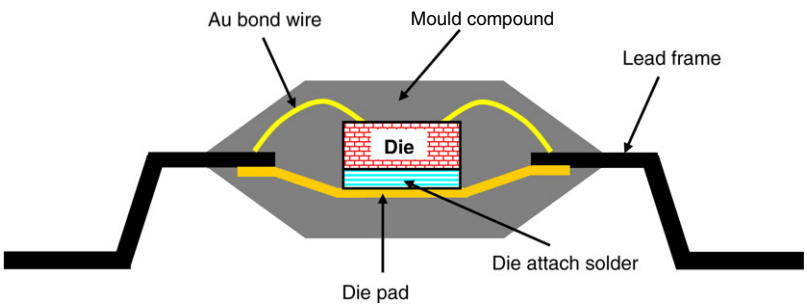

Figure 11. Cross-section of Quad-Flat package (QFP).

performance is improved by decreasing the X or by increasing the X_C value.

The improvement of one factor will probably worsen other factors. The improving direction of material properties is package dependent. One type of material improvement will not be always suitable for any package, e.g., moulding compound of low coefficient of thermal expansion (CTE) is desired in most of the packages, but the low CTE may make the situation worse in some package with substrate of large CTE. Decreasing the CTE of moulding compound through increasing the filler content is often employed to reduce the warpage and stress, but the high filler content will always increase the modulus of the compound, which will induce larger local stress in the same CTE mismatch or the same warpage, and will perhaps worsen the delamination. The advantage of increasing filler content is to decrease stress though lowering the CTE mismatch and the disadvantage of increasing filler content is to increase stress induced by higher modulus. In view of the above, the change is adopted only when the stress decrease induced by lower CTE mismatch exceeds the stress increase induced by higher modulus. Other effects of changing filler content should also be taken into account, such as worse mould ability, worse flow ability, worse wire sweep and worse void performance. Only the improvement modality in which the advantage accrued counterpoises the accompanied disadvantage, or of which the disadvantage is constrained within the accepted scope, is implemented.

Over the recent years, Sn-rich solders have aroused significant interest as suitable substitutes for Pb-bearing solders. Typical pad metallizations include Ni–Au, Cu,

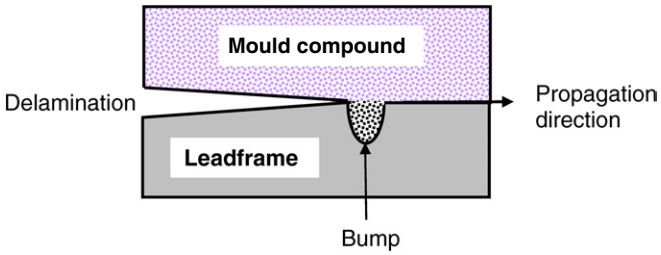

Figure 12. Retardation of delamination by bump.

or Ni–Pd. Reflowing of Sn-rich solders on such pad metallizations, leads to the formation of several intermetallics, e.g., Cu_6Sn_5, Ni_3Sn_4, Cu_3Sn and Ag_3Sn. While the presence of these intermetallic compounds promotes proper bonding and adhesion between the solder and metallization, large thicknesses of the intermetallic layer noticeably lowers the fracture toughness of the joint. Furthermore, the reliability of Sn-rich solders is degraded in cases of high strain loading. Failure analysis of the solder joint shows that fracture takes place at the intermetallics [89]. The critical thickness of Ni_3Sn_4 resulting in intermetallic compound failure instead of bulk solder failure is approximately 1.5–2.5 μm. The critical thickness for the same effect of Cu_6Sn_5 solder is 4–6 μm. Observation of the fracture toughness behaviour showed that toughness decreases by as much as 22% when failures shift from the bulk solder to the intermetalllic compound. For a given thickness, the fracture toughness of Cu_6Sn_5 is greater than that of Ni_3Sn_4. However, Cu_6Sn_5 experiences more rapid growth with extended exposure to reflow. A large decrease in toughness is produced.

A bumpy interface works as the retardant of delamination propagation (figure 12) [80]. It is the change in the propagation direction in the structure with bumpy interface that works as the retardant. The bumpy interface is less likely to crack than the even surface.

Copper leadframe enhances the adhesion with the moulding compound. The existence of a small amount of cupric oxide (CuO) was observed next to the Cu_2O, which corroborated the oxide layer structure of $Cu/Cu_2O/CuO/air$. The incipient stage of oxidation improved the adhesion strength between moulding compound and Cu leadframe. The optimum copper oxide thickness producing the maximum pull strength ranged from 20 to 30 nm. Presumably, the high pull strength was due to the increase in surface wettability and mechanical interlocking effects resulting from oxidation ('–O' in leadframe surface and '–OH' from moulding compound form hydrogen bond, which increases the adhesion strength.). It was also reported by Bischof [91] that oxidized leadframes far out-performed the other leadframes on both tab adhesion and percentage delamination testing. The extraordinary adhesion to the oxidized leadframe originated from the mechanical bonding of the moulding compound to the rough shredded-wheat-type finish of the oxide.

Moisture has a great impact on the reliability of a plastic package. Electronic packages absorb water. The moulding compound expands after absorbing moisture, and the moisture expansion is termed *hygroswelling*. It persuades the deformation mismatch between the compound and other parts in the plastic package.

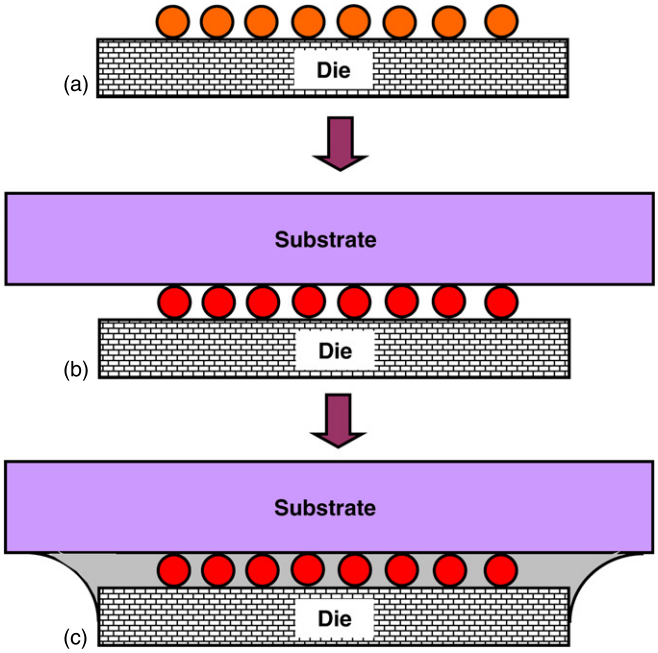

Figure 13. Flip-chip packaging: (*a*) solder bumping, (*b*) solder reflow and (*c*) underfilling and thermal cycling.

The vapour pressure created by high temperature of solder reflow induces the delamination propagation, even popcorn cracking. During the high temperature soldering process, the absorbed water vaporizes creating high internal stress. This stress causes delamination at the interface between the chip and the epoxy moulding compound. Delamination in turn leads to cracking of the epoxy moulding compound. This is eventually a serious reliability and functionality concern because it damages the circuit and ushers catastrophic corrosion-related failures. The above result is typical of the loss of interfacial fracture toughness strength during the soldering process. The moisture causes the interface adhesion strength between moulding compound and substrate, leadframe and die to deteriorate.

9.2. Flip-chip packages and anisotropically conductive films (ACFs)

Flip-chip microelectronic assembly is the direct electrical connection of face-down (hence, 'flipped') electronic components onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip bond pads (figure 13). Exclusion of packages and bond wires reduces the required board area by as much as 95%, and requires far less height. Flip chip is the simplest minimal package. The absence of bond wires decreases the delaying inductance and capacitance of the connection by one order of magnitude, and shortens the path by a factor of 25–100, resulting in high-speed off-chip interconnection. Flip chips, when completed with an adhesive 'underfill,' are solid little blocks of cured epoxy. They are mechanically the most rugged interconnection embodiments. The flip-chip assembly method involves three stages: bumping

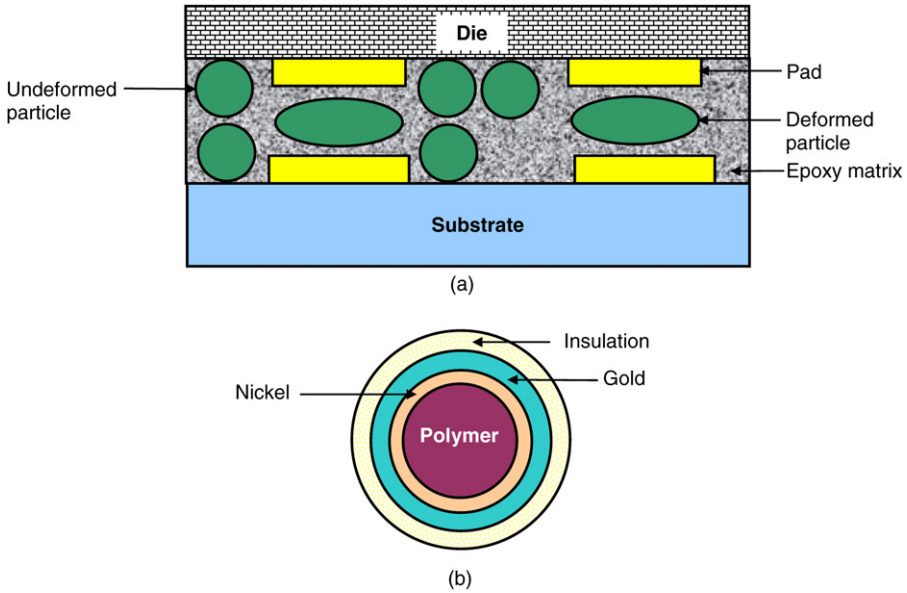

Figure 14. (*a*) Flip-chip bonding using ACF. (*b*) Structure of conductive particle.

the die or wafer, attaching the bumped die to the board or substrate and filling the remnant space under the die with an electrically non-conductive material.

In order to realize an electrically conductive connection in electronics, solder still plays the central role because of its well-tested, well-known properties, reliable production equipment developed for soldering and low and stable contact resistance. But recently, interest in the use of *electrically conductive adhesives* is growing in applications that were traditionally reserved for solders. Benefits of *adhesive technologies* are compatibility with a wide range of surfaces including non-solderable surfaces; low temperature processing ($<150\,^{\circ}$C); low thermal stress during processing; improved thermomechanical performance: less brittleness on long-term exposure to high temperature, less sensitivity to fatigue; a thermosetting feature preventing reflow in subsequent assembly steps; the absence of residuals; high surface insulation resistance; reduced pre-clean or post-clean requirements; non-requirement of cleaning agents or washing equipment; non-appearance of Pb or other toxic metals; finer pitch capability and elimination of solder mask requirement.

Flip-chip joining technology using anisotropically conductive films (ACFs) has become an attractive technique for electronic packaging (figure 14) [88]. ACFs consisting of an epoxy matrix and dispersed conductive particles offer suitable alternatives to solder because they enable ultrafine pitch capability, and are lead free, therefore environmental friendly.

Interconnects using ACFs show excellent reliability for the noble metallization surfaces, such as gold-to-gold interconnection. Adhesion strength of ACF with the Al metallization was increased during $60\,^{\circ}$C/95% RH testing. After 500 h of such moisture-soak testing, the adhesion strength became 3 times the initial value. The higher adhesion strength was ascribed to change in chemical state on the aluminium surface [82]. It was proposed that oxidation of the Al surface due to diffused moisture and the new chemical bond formation at the adhesives/aluminium interface were the factors responsible for good adhesion reliability. Chemical reactions were proposed between the oxygen-containing radical of epoxy and aluminium that contribute to the increase in adhesion strength. These alphatic chains and networks protect the interface from further contact with free water. There were no cracks or voids found at the ACF to the Al metallization interface. Hence the adhesion strength increased between the ACF matrix and aluminium metallization.

9.3. Multilayered flexible electronics

Multilayer materials consisting of base polymers with a variety of applied layers are widely used as flexible substrates in display applications [88]. A flexible substrate is often mantled on both sides with an inorganic/organic hybrid layer that not only acts as a gas barrier but also increases the scratch resistance. Such a layer is called a *hard coat* (HC). On top of the hard coating, a transparent conducting oxide layer such as indium tin oxide layer (ITO) is applied. Buckling-driven delamination of thin film structures is noticed in these substrates. From an initial region of weak adhesion between film and substrate, buckling-driven delamination of the film is observed to take place through compressive stresses. The coupling of buckling and interfacial delamination is the reason behind this failure mode. The occurrence of these phenomena is undesirable from functional and reliability points of view and should therefore be subdued.

9.4. Other adhesion-related problems in packaging

Wafer backside contamination-induced package interfacial delamination needs in-depth treatment [73, 74]. Wafer tape is extensively used during the packaging assembly process. It serves as a structural support for the wafer for chip dicing. Afterwards, it holds the separated chips during the lead frame bonding operation, preventing the chips from falling apart.

Following the completion of the dicing process, the chips are removed from the supporting wafer tape. The wafer tape composition includes an adhesive, a base film and a release liner. Application of the wafer tape to the backside of a wafer is followed by its exposure to ultraviolet radiation to start a chemical reaction in the tape adhesive. The components of the tape adhesive and the UV-induced reactions determine the final properties of the tape adhesive. The tape adhesive is generally 5–15 μm thick. It is typically composed of five components: a *base polymer*, which is the principal structural element of the adhesive; an *anoligomer*, which adjusts the adhesive strength and hardness so that the chips are readily removed from the tape; a *cross-linking agent*, intended to enhance the cohesion of the adhesive by inducing bonding among the base polymer chains; a *photoinitiator* for enhancing the degree of bonding by creating radicals during the UV exposure; and an *additive agent*, which does not chemically react with the other components but is used to modify the adhesive strength independently of the oligomer. The chip surface characteristics affecting interfacial adhesion must be taken into account to eliminate the interfacial delamination between the chip backside and the moulding resin. Delamination failures are less likely to occur with higher elastic moduli adhesives. More specifically, adhesives with elastic moduli in excess of 1000 MPa exhibit no interfacial delamination. It is believed that an adhesive with a high elastic modulus has good cohesion strength, and therefore leaves scanty adhesive fragments on the chip backside surface. From these arguments, the criteria for eliminating backside delamination were standardized as follows [73]: an elastic modulus >1000 MPa, a contamination of <500 particles/half wafer and a water contact angle of $<50^\circ$ (moderately hydrophilic). These adhesive criteria are utilized for developing new wafer tape adhesives designed to eliminate backside delamination in electronic packages. Adhesives with a high elastic modulus eradicated contamination. Concurrently, they improved the wettability of the chip backside surface resulting in reduction of interfacial delamination and cracking in electronic packages

An important interface in electronic packages is the *epoxy resin to the polyimide surface* [73]. The common failure mode is delamination or cracking around this interface between dissimilar materials. The interface is characterized by its *stress intensity factor*. Obviously, the prediction of delamination and cracking depends on an understanding of the critical stress intensity factor. In addition, improvement of interfacial adhesion at the polyimide-coated chip surface depends on an understanding of the interactions between moulding compound and the polyimide. The critical stress intensity factor is mainly governed by the polyimide surface micro-roughness. The molecular chains of the epoxy moulding resin bind to the micro-rough polyimide surface through hydrogen bonding between the hydroxyl groups of the epoxy resin and the oxygen atoms of the polyimide surface, and the orientation of polyimide molecular chains. After the C–N, C–C and C–O bonds are easily broken under the process conditions, the degrees of freedom for molecular motion for the C_6H_6 bond, the O=C–N bond and the C=O bond are increased. As a result, a strongly hydrophilic surface is produced with an augmented density of carbonyl and carboxyl groups. The surface micro-roughness obtained with the higher density of carbonyl and carboxyl groups elevates the critical stress intensity factor and interfacial adhesion. The polyimide molecules were oriented at 30–40° against the polyimide surface. The imide chains were oriented at 5–25° against the polyimide surface. These orientations led to increased degrees of freedom of molecular motions, rendering the surface more wettable and also the interfacial adhesion stronger.

Some examples of specific stress and adhesional problems and their solutions are as follows:

(i) Yeung and Yuen [92] examined the influence of variation of processing conditions on warpage prediction of a plastic quad flat package (PQFP). Residual stress in IC packages evolves from volume shrinkage due to cure reaction and thermal stress. Volume shrinkage of cure compound is dependent upon pressure, temperature, time and degree of cure. The degree of cure (DOC or β), coefficient of thermal expansion (CTE or α), glass transition temperature T_g and shear modulus G' and G of the moulded specimens were measured by various thermal analysis techniques. Using finite element analysis techniques, package warpage predictions against different processing conditions were performed. Agreement of warpage prediction with the measured data by the viscoelastic material model was found to be closer than obtained by applying the thermoelastic one. For a given cured content, less warpage was found in packages moulded at low temperature and longer moulding time or high temperature and shorter moulding time.

(ii) Koganemaru *et al* [93] measured the actual residual stress of the packaging process by using test chips that included piezoresistive gauges. A *linear thermoelastic finite element analysis* was then carried out using a three-dimensional model. The measured residual stress using the test chips matched well with the results of the finite element analysis. In this work, two types of resins having different CTEs were used for the moulding: resin A and resin B. The residual stresses on the surface of the semiconductor chip in the QFP obtained from the experiments were found to be compressive 80 MPa for resin A and compressive 160 MPa for resin B. The CTE of resin B was 2.5 times that of resin A. On the other hand, the residual stress on the surface of the semiconductor chip in the QFP with resin B was twice that with resin A. This explained that the higher residual stress in the QFP with resin B was caused by the higher CTE of this resin. In this way, residual stresses in packages are determined and correlated with delaminations.

The literature is replete with such examples [94–98].

10. Discussions and remedial measures

Microelectronics and MEMS structures comprise multiple layers of materials with interfaces between them. Although a fundamental understanding of the effects of environment and loading conditions on interface integrity is an important

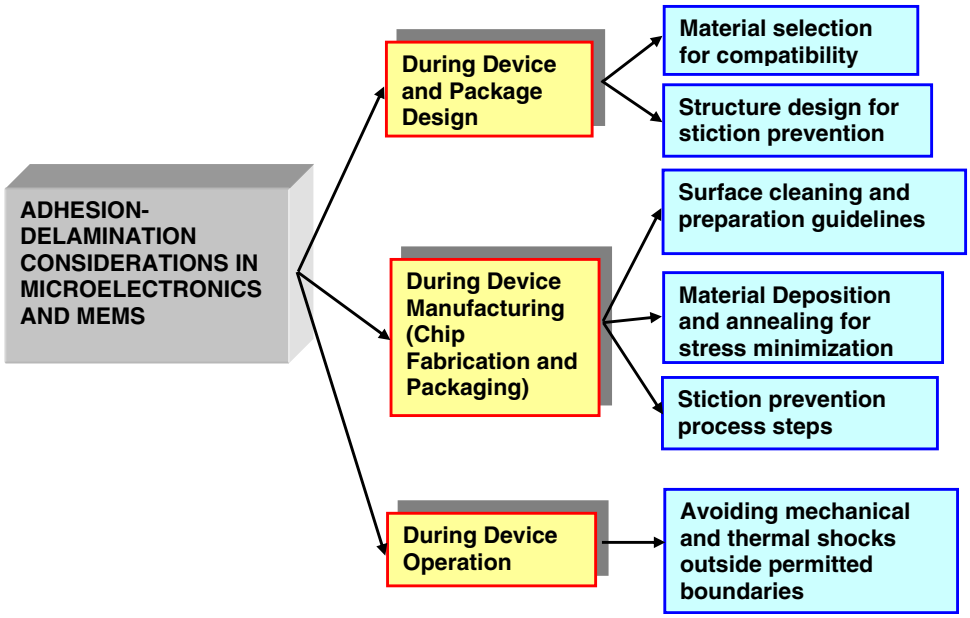

Figure 15. Planning for elimination of adhesion–delamination problems in microcomponent fabrication and packaging.

parameter in device design, there are only a limited number of studies that have addressed debonding. To secure proper adhesion at these interfaces, it is prudent to envisage the likely failure causes and plan the strategy from the beginning itself.

Microelectronic/MEMS devices are used in a variety of environments (household, industrial, low earth orbit, etc) where they are susceptible to attack by environmental species and are subjected to thermal and mechanical loading produced both internally (thermal cycling during use, residual stresses) and externally (thermal fluctuations in the environment, vibration, shock). During operation, the device makes several thermal excursions and during this temperature cycling, delamination may occur. There are different mechanisms from which delamination starts, i.e. mismatch in Poisson's ratios, difference in coefficients of thermal expansion (CTE) and in-plane shear stiffness mismatch. The first and foremost issue is material selection to ensure mutual compatibility with regard to physical parameters such as coefficient of thermal expansion and moduli of elasticity, i.e. Young's and shear modulus. In the case of crystalline materials, lattice mismatching should be avoided. A compromising or trade-off solution is only possible because of conflicting requirements of interfaces. But the best optimization must be made.

Another consideration in choosing materials is to take note of their intermixing behaviour as determined by enthalpy of formation. Gold has problems adhering to SiO_2, but there are established methods to circumvent them. One method employed is to use an intermediary layer of chromium as an adhesive, since it forms chromium trioxide (Cr_2O_3) with SiO_2 and also strongly bonds to gold. Because aluminium forms aluminium oxide (Al_2O_3) bonds with SiO_2, it is simple to adhere it to passivation layers. Copper does not adhere well to silicon, which makes it likely to delaminate. The ability of copper to find a niche in the MEMS community will largely hinge upon the strength of the adhesive bonds that can be formed.

Even if the materials are carefully selected, it is unreasonable to expect that delaminations will not take place because material deposition parameters must be standardized for stress minimization. Materials must be deposited at medium rates to allow the nucleation, spreading and coalescence of molecules to form surfaces. After reaching the surfaces, the atoms do not possess adequate kinetic energies to reach the lowest energy states before arrival of more atoms resulting in non-equilibrium atomic arrangement, which is frozen in as a stressed condition. Faster deposition rates generally tend to create stresses but equipment throughput is also vital.

Residual stresses in films may initiate cracks and delaminations if left as such. Hence, any residual stresses left in the materials have to be annealed out by subjecting the deposited material to temperature treatment.

Needless to say that cleaning and surface preparation procedures must be stringently followed otherwise all endeavours will be wasted. Besides chemical cleaning, argon sputtering and plasma processing must be resorted to as deemed necessary. UV exposure helps in removing photoresist residues.

MEMS devices need additional attention. In MEMS devices, surfaces vulnerable to stiction must be identified and precautionary measures should be taken at the time of device design in terms of detachment lengths and minimizing the area of contact by incorporating bumps on the surfaces. Also, care must be taken during releasing and drying the suspended structures to prevent their adhesion to surfaces in proximity by receding water films during evaporation. Techniques such as the freeze-drying method, supercritical drying, dry etching of sacrificial films and liquid-bridge cleavage must be employed to circumvent the adhesion effects in drying of MEMS structures.

In packages, the interfaces at risk are those between wire and lead, lead and compound, die attach and

diepad, IC and compound, etc, notably the solder joint interconnects, the polymer die attach material interface, the epoxy moulding compound–silicon chip interface, the epoxy moulding compound chip coated polyimide interface and the epoxy moulding compound-die pad. Malfunctioning occurs through different types of failure modes, such as cracking (passivation, package body, etc) and/or metal fatigue (wires, solder connections, etc). Careful material choice with regard to material compatibility is mandatory in packaging also. Moreover, steps to improve adhesion between surfaces such as by proper surface preparation, roughening, etc must be practiced.

During the operation of microelectronics and MEMS devices, thermal and mechanical shocks beyond specified limits should be avoided because they are the activators of cracks and delaminations. Moisture absorption and its penetration is another factor so that ambient humidity must be maintained within permissible limits [99, 100]. A proper environment must be provided for the device to achieve the targeted performance.

Adhesion–delamination considerations are summarized in figure 15.

11. Conclusions and outlook

A diversity of phenomena related to adhesion and delamination in IC and MEMS manufacturing were elaborated. The structures of these devices contain several sites of *desired adhesion* where adhesion must be secured and also those of *undesired adhesion* at which it needs to be weakened. Understanding of these phenomena and implementation of corrective measures is an essential prerequisite for guaranteeing satisfactory operation of devices during their lifetime as well as for their longevity. There is a strong desire from the microelectronics industry to understand, control, possibly predict and eliminate these kinds of delamination failures. Researchers worldwide are continuously addressing these areas. The microelectronics industry push towards the nanoscale has provided the driving force for acquiring a better understanding of adhesion physics. The science of adhesion is a multidisciplinary realm embracing both chemistry and physics.

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